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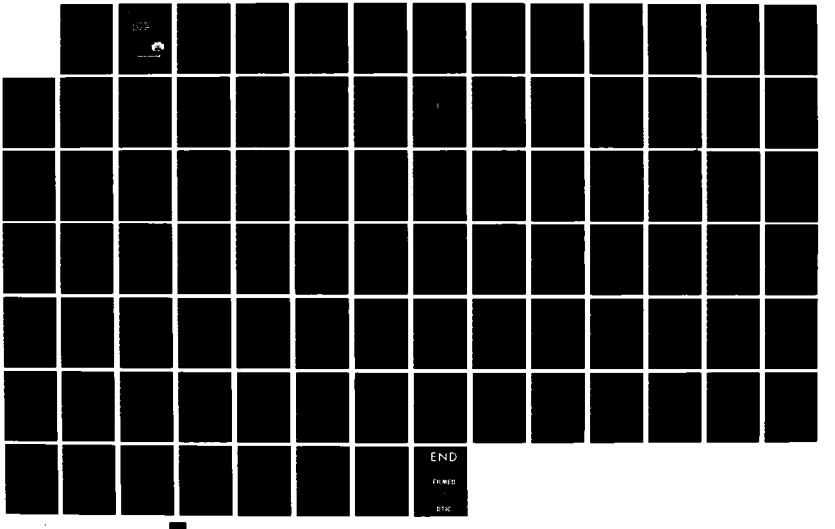

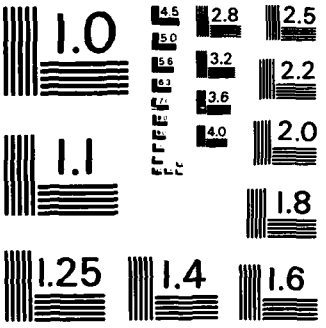

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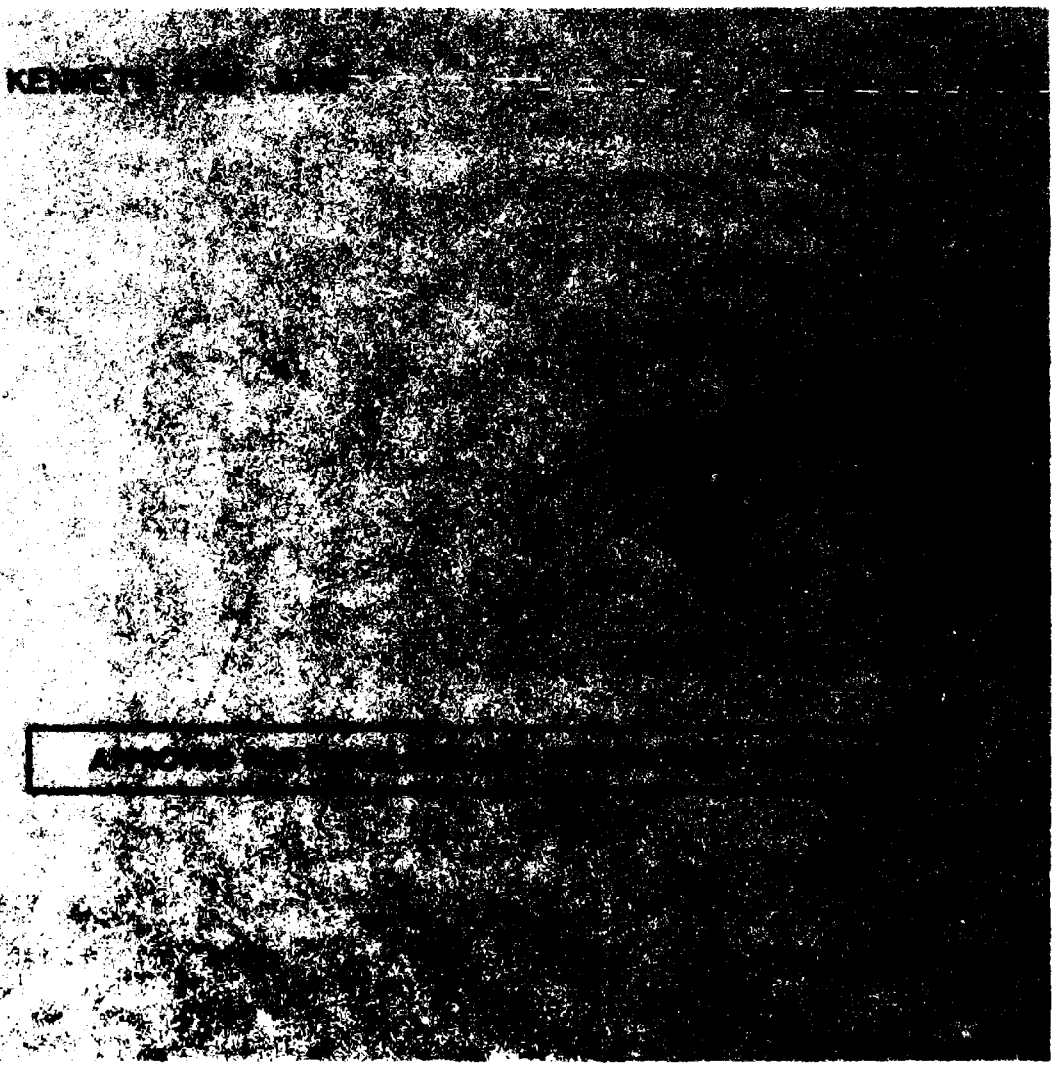
COORDINATED SCIENCE LABORATORY

A PIECEWISE-LINEAR APPROACH TO TRANSIENT ANALYSIS OF LARGE-SCALE INTEGRATED CIRCUITS



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A Gauss-Seidel waveform relaxation method is described for time-domain analysis of piecewise-linear circuits. The method relies on approximating both the nonlinear element characteristics and the voltage (or current) waveforms by piecewise-linear functions; and is suitable for timing analysis of large-scale integrated circuits.

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A PIECEWISE-LINEAR APPROACH TO TRANSIENT ANALYSIS OF LARGE-SCALE INTEGRATED CIRCUITS

BY

KENNETH KAM JUNG

B.S., Arizona State University, 1981

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical Engineering
in the Graduate College of the
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TABLE OF CONTENTS

Chapter 1

INTRODUCTION

The properties of metal-oxide-semiconductor (MOS) field effect transistors, namely, high circuit packing density, low power dissipation, simplified processing, and therefore, low cost, have made Very Large Scale Integration (VLSI) a reality. The integrated circuit in which thousands of transistors may be fabricated in a single monolithic chip has added a new dimension to electronic circuit analysis. In addition, the complexity and long term reliability requirements of VLSI chips, such as RAM's, require their design to be very nearly optimum in relation to both circuit and device processing. Also the designs of custom logic array demand a high degree of accuracy. One reliable method of achieving the above design goal is through the use of circuit simulation programs. The correct correlation between the computer simulated results and experimental measurements, however, depends primarily on two important factors. The first is the accuracy of the computational method used in the simulation; the second is the accuracy of the modeling technique used in characterizing the devices in the circuit.

As the number of transistors in the circuit increases, simulation which can accurately predict circuit performance becomes very expensive. The two major limitations are the computer storage capabilities and computer time requirements. Therefore, the determination of the solutions in circuit

analysis is important not only from a circuit-theoretic point of view but even more so from a computational point of view. This research is concerned with the development of a piecewise-linear model and some waveform approximation techniques for fast and relatively accurate time-domain simulation of MOS LSI circuits. The results are found to be comparable in accuracy to those obtained by SPICE2 [1], which in fact will be used for comparison purposes.

The iterative piecewise-linear (PWL) method [2] is used for analysis and modeling of the MOS devices. The basic philosophy of the iterative PWL method consists of treating a nonlinear network as if it was a number of distinct linear networks having identical network topology. Each linear network can then be analyzed independently by simple linear techniques. This is possible because by assumption the i-v curves of all nonlinear elements can be realized by PWL segments. Based on this philosophy, a PWL model for the MOS device, which consists of an interconnection of two-terminal elements [3], is constructed and studied.

As a result, the model as presented here is in a form most suitable for easy table lookup technique. The advantage of generating tables of device characteristics prior to the analysis is to replace the expensive analytic function evaluations with simple table lookups. Although these tables may occupy more memory space than the analytic functions, this penalty can be justified in terms of the speedup in computation.

The technique of PWL function generation involves approximating the i-v curve of the model's two-terminal elements with continuous straight-lines segments. It is easy to see that, by increasing the number of segments, a PWL function can represent the actual curve to a high degree of accuracy. However, more segments will be penalized on more memory space for more table entries and longer computation time for more breakpoint detection [4]. For practical purposes, it has been found that a three-segment PWL approximation gives acceptable accuracy in digital circuit simulation. Since there is no general method to find the best approximation of the i-v curves by segments, the input-output characteristics of an inverter will be used to investigate the accuracy. The Katzenelson technique [5, 6] will be employed for obtaining the DC operating points. The transient behavior of the inverter is studied for model validation. A multiple-input NAND gate is used to study the effects of a floating node caused by stacking up transistors. Initially, a step input waveform is applied during the analysis to study the effects of the MOS model parameters on the accuracy of the results. It is well-known that the step response of a linear first-order RC circuit is exponential with the time constant equal to RC [7] . This simple observation is the key to the development of simulation techniques developed in this thesis. In practice, the constant step input is not very realistic. In most cases, the signals are not step functions, which, as will become obvious later, tend to slow down the simulation

method proposed in this thesis. For this reason, two methods are used to approximate general waveform functions: discrete stepwise approximation and PWL continuous (ramp) approximation. A Gauss-Seidel Waveform Relaxation (WR) method [7] will be used to decouple the circuit equations into a sequence of first-order piecewise-linear differential equations.

Chapter 2 describes briefly the PWL transistor model and its features for table lookups. Chapter 3 discusses the function generation by PWL approximation. Chapter 4 examines the transient behavior of the model and presents simple solutions of the step response in normal form. Chapter 5 illustrates the results with simple stepwise waveform representation and suggests an alternative approach to represent the waveform which could lead to variable step size approach. In the final chapter, conclusions are presented and areas for future work are suggested.

Chapter 2

DEVICE MODELING FOR MOS

2.1 Introduction

In circuit simulation, a simple MOS model capable of producing accurate solutions at high computational speed is very desirable. Hence, the device physics level modeling is impractical for the application in VLSI circuits, even though in principle the resulting circuit model would be extremely realistic. Although no general theory of device modeling is presently available, the transistor DC characteristics are usually represented by nonlinear polynomial (quadratic) functions [8]. This representation will be referred to as the "functional" model. In this thesis, the characteristics will be approximated by a PWL continuous function. This approximation will be referred to as the PWL model.

In Section 2.2, the "functional" model is presented which will form the basis for the development of the PWL model. In Section 2.3, the relationships between the configuration of the model and table lookups are discussed. In Section 2.4, the elements of the PWL model are shown.

2.2 Functional Model

Without loss of generality, the NMOS transistor will be used for illustrative purposes throughout this thesis. The basic Sah model [8] is adopted as the functional model which

gives analytical expressions for the NMOS. This simplifed version of Sah's model has been derived from a circuit design standpoint, considering the device parameters which are important in the design of MOS integrated circuits. As a practical matter of VLSI circuit simulation, normal values and statistical variations of the threshold voltages, body-effect coefficient, and temperature sensitivity are not included. The special geometrical feature of a short-channel device usually requires a separate model from the long-channel device; this model does not include the short-channel effect. The device symbol which represents an n-channel enhancement type transistor is shown in Fig. 2.1.

The mathematical equations for the channel current in the triode (non-saturation) and saturation regions are given as follows:

Nonsaturation Region:

$$I_{DS} = K\left[2(V_{GS}-V_T)V_{DS}-V_{DS}^2\right] \quad 0 \leq V_{DS} \leq V_{GS}-V_T \qquad (2\text{-}1)$$

Saturation Region:

$$I_{DS} = K(V_{GS}-V_T)^2 \qquad 0 \leq V_{GS}-V_T \leq V_{DS} \qquad (2\text{-}2)$$

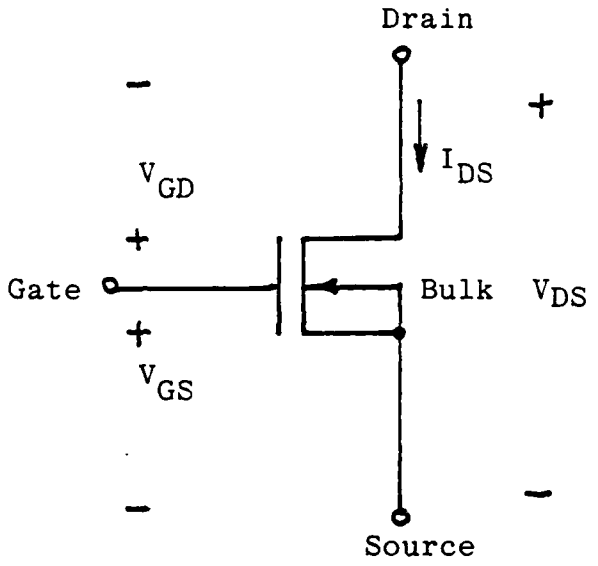


Fig. 2.1. Device symbol for NMOS transistor.

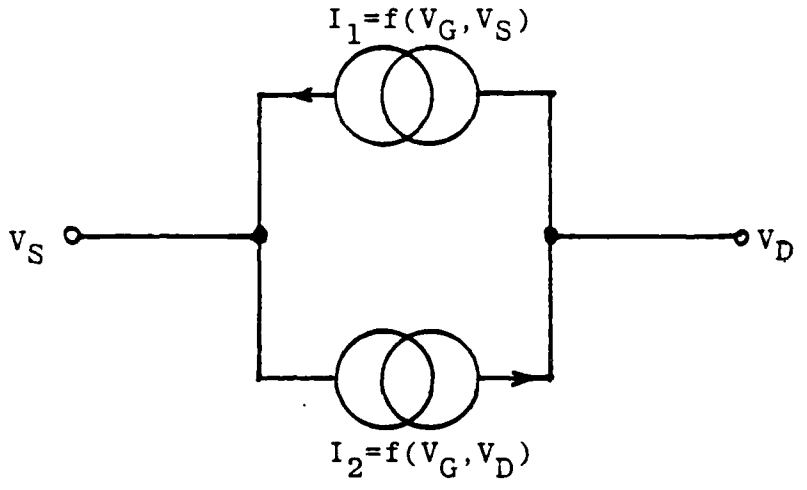


Fig. 2.2. Two-current source MOS model.

The constant K is given by

$$K = \frac{\mu \varepsilon_{ox}}{2t_{ox}} \frac{W}{L} \tag{2-3}$$

where μ = average surface mobility of carriers in channel (electrons in n-channel) devices

ε_{ox} = permittivity of the oxide insulting layer

t_{ox} = thickness of oxide under gate

L = length of channel

W = width of channel

The V_{GS}, V_{DS}, and V_T are gate to source voltage, drain to source voltage, and threshold voltage, respectively. Two parameters are defined as KP and k for convenience. The transconductance parameter KP is defined as

$$KP = \frac{\mu \varepsilon_{ox}}{t_{ox}} \tag{2-4}$$

The width-to-length ratio of channel, k, is given by

$$k = \frac{W}{L} \tag{2-5}$$

If the table lookup method was used to solve the given mathematical equations, a straightforward approach would require a 2-dimensional table, T_d, to obtain the channel current.

$$V_{GSE} = V_{GS} - V_T \tag{2-6a}$$

$$I_{DS}(V_{GS}, V_{DS}) = T_d(V_{GSE}, V_{DS}) \tag{2-6b}$$

However, the number of entries for the 2-dimensional table

may offset the advantage of evaluation time. One-dimensional tables which reduce both memory requirements and model evaluation time are proposed in the next section.

2.3 Equivalent Circuit Model with 2-Terminal Elements

As shown later, 1-dimensional tables achieve considerable memory savings as compared to 2-dimensional tables. One approach is to use two 1-dimensional tables [9] in the following form:

$$I_{DS}(V_{GS},V_{GD}) = T_e(V_{GS}) + T_f(V_{GD}) \qquad (2\text{-}7)$$

The above form is feasible by noting that the nonlinear relationships between channel current and the terminal voltages can be written as the difference between two nonlinear current components, each of which is dependent on only one pair of terminal voltages [10].

$$I_{DS} = I_1 - I_2 \qquad (2\text{-}8)$$

where $I_1 = K * f(V_G,V_S)$

$I_2 = K * f(V_G,V_D)$

The form with two current components is easily generated by substituting V_{DS} with $V_{GS}-V_{GD}$ into Eq. (2-1). The final form is given by [10].

$$I_{DS} = K(V_{GS}-V_T)^2 - K(V_{GD}-V_T)^2 \qquad (2\text{-}9)$$

Thus, $f(V_G,V_X)$ has the following conditions:

$$f(V_G,V_X) = [(V_G-V_T) - V_X]^2 \quad \text{for} \quad V_G-V_T > V_X \qquad (2\text{-}10a)$$

$$= 0 \qquad \text{for} \quad V_G-V_T < V_X \qquad (2\text{-}10b)$$

The configuration of two current sources is illustrated by the model of Fig. 2.2.

Proceeding one step further, an approach dealing with interconnections of 2-terminal circuit elements yields the Ebers-Moll "like" model of Fig. 2.3. Both forward and reverse α's must equal unity in order for the gate current $I_g = 0$, as it must be for an MOS transistor. The i-v characteristics of the diode element are as described by Eq. (2-8) and Eq. (2-10). The given conditions of $f(V_G,V_X)$ enable Eq. (2-8) to represent the channel current in both regions with $I_2 = 0$ in the saturation region and exhibit the familiar quadratic characteristics. The completely bidirectional feature of the model also reduces the two 1-dimensional tables to one.

2.4 Elements of PWL Model

A one-dimensional PWL function can be represented mathematically by

$$y = m_j x + k_j \qquad a_j \leq x \leq b_j \qquad j = 1,2,... \qquad (2\text{-}11)$$

The linear function defined in each interval of Eq. (2-11) will be called segment, and the endpoints of each segment will be called breakpoints. A set of four parameters (m_j,k_j, a_j,b_j) is required to describe each segment. After the setup of the PWL segments, an equivalent circuit consisting of linear

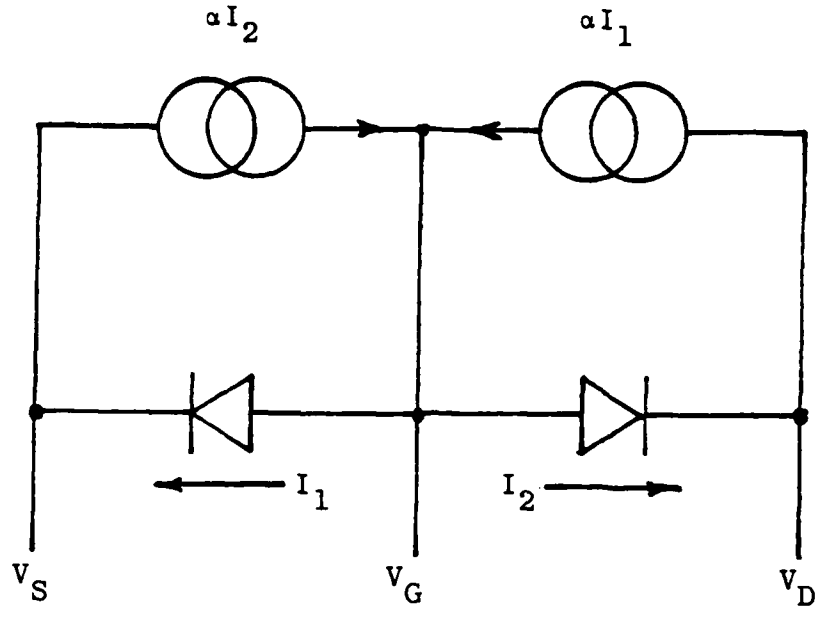


Fig. 2.3. Ebers-Moll "like" MOS model.

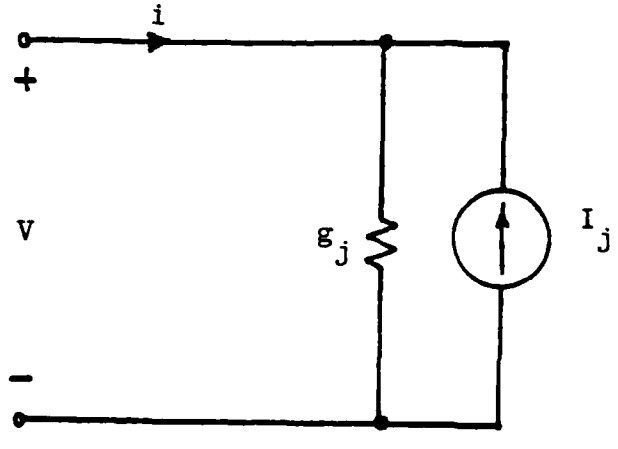
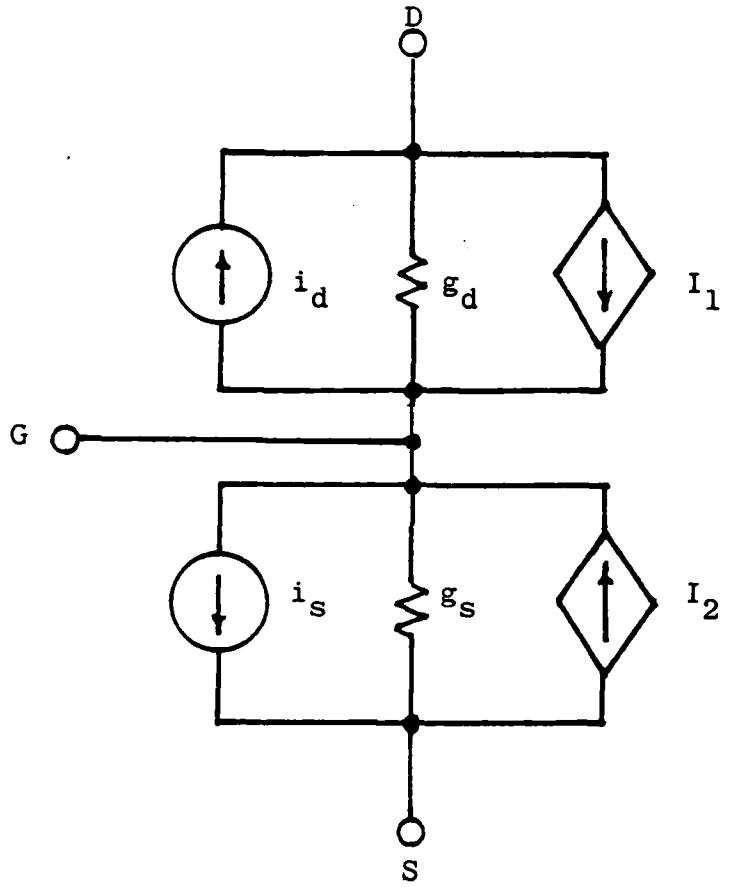


Fig. 2.4. Norton equivalent circuit for PWL segment.

elements and independent sources could be used to represent the curves in a given region.

The i-v curve characterized by Eq. (2-10) will be approximated by PWL segments. Let g_j be the slope of segment j in the PWL representation. Let segment j or its extension intersect the i-axis at I_j. Let segment j be defined for all $a_j < v < b_j$. Within the prescribed intervals for segment j, the characteristics can be replaced by the Norton equivalent circuit of Fig. 2.4. The conductance is used to realize the slope of the segment and the independent current source is used to represent the i-axis intercept. In order to keep the gate current $I_g = 0$, as it must be for MOS, two linear controlled current sources are added to implement this physical property. As a result, a PWL model is constructed as shown in Fig. 2.5. It is also noted that the completely bidirectional feature of the MOS devices gives the identical i-v characteristics for the two nonlinear resistors. Hence, the parameters needed to describe the segments are tabulated only once.



$I_1 = V_{GS}*g_s+i_s$

$I_2 = V_{GD}*g_d+i_d$

Fig. 2.5. Piecewise-linear model for MOS.

Chapter 3

PIECEWISE-LINEAR FUNCTION GENERATION

3.1 Introduction

The linear function defined In Eq. (2-11) formulates many segments and breakpoints. It is easy to see that, by increasing the number of segments, a piecewise-linear function can represent the actual function to a high degree of accuracy. However, four parameters are required to describe each segment. More segments will require more memory space for more table entries and also longer computational time for more breakpoint detection. For digital circuit applications, we found that a three-segment PWL representation with appropriately chosen breakpoints gives acceptable solutions when compared to SPICE2.

Without any loss of generality, the standard depletion-load inverter will be used for accuracy measurement. The device symbol for the inverter is shown in Fig. 3.1. The following parameters of the inverter will be used throughout this thesis. Let k_D and k_L be width-to-length ratios of the channel for the driver and the load, respectively. Let V_{TD} and V_{TL} be the threshold voltage for the driver and the load, respectively. The transconductance parameter KP is set to the default value of SPICE2 at 20 $\mu A/V^2$. Typical values of 1 V and -2 V are used for the threshold voltages of the enhancement and depletion transistors, respectively. The power supply V_{plus} is 5 V. Base on the minimum gate area criterion

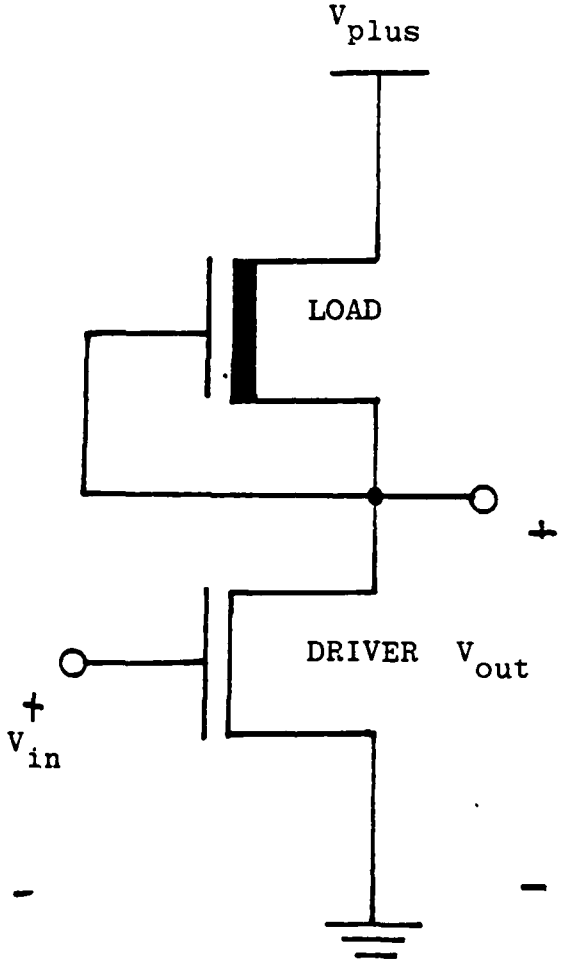


Fig. 3.1. Depletion-load inverter.

and an arbitrary value of 0.2 V for solid logic "0", k_D and k_L have values of 1.60 and 0.625, respectively. The PWL model for the inverter is shown in Fig. 3.2.

3.2 Approximation by Chord

One straightforward approach to generate a piecewise-linear function is to connect a set of sampling points with straight line segments [4]. The i-v curves of the nonlinear resistors with 3-segment approximation are shown in Fig. 3.3. After the setup of the segments, the four parameters (m_j,k_j, a_j,b_j) are tabulated in Tables 3.1(a,b).

In order to measure the accuracy of the segment approximation, the Katzenelson techniques will be used to find the DC operating points of the inverter. Results from the analytical method on the functional model will be used for comparison. Analysis of the functional model gives the switching point where input V_{in} is equal to output V_{out} at 2.25 V. In other words, V_{out} is expected to have a high value when V_{in} is less than 2.25 V and vice versa.

The active range (-2 V to 0) of the depletion transistor is relatively short. Hence, two segments with equal intervals provide a good approximation. More attention was placed on the selection of the breakpoint V_z on the longer active range (1 V to 5 V) of the enhancement driver. Selecting the wrong V_z will result in unrealistic solutions. This problem can be demonstrated by considering the case where $V_{in} < 2.25$ V and $V_z > 2.25$ V. The expression of output V_{out} at the output

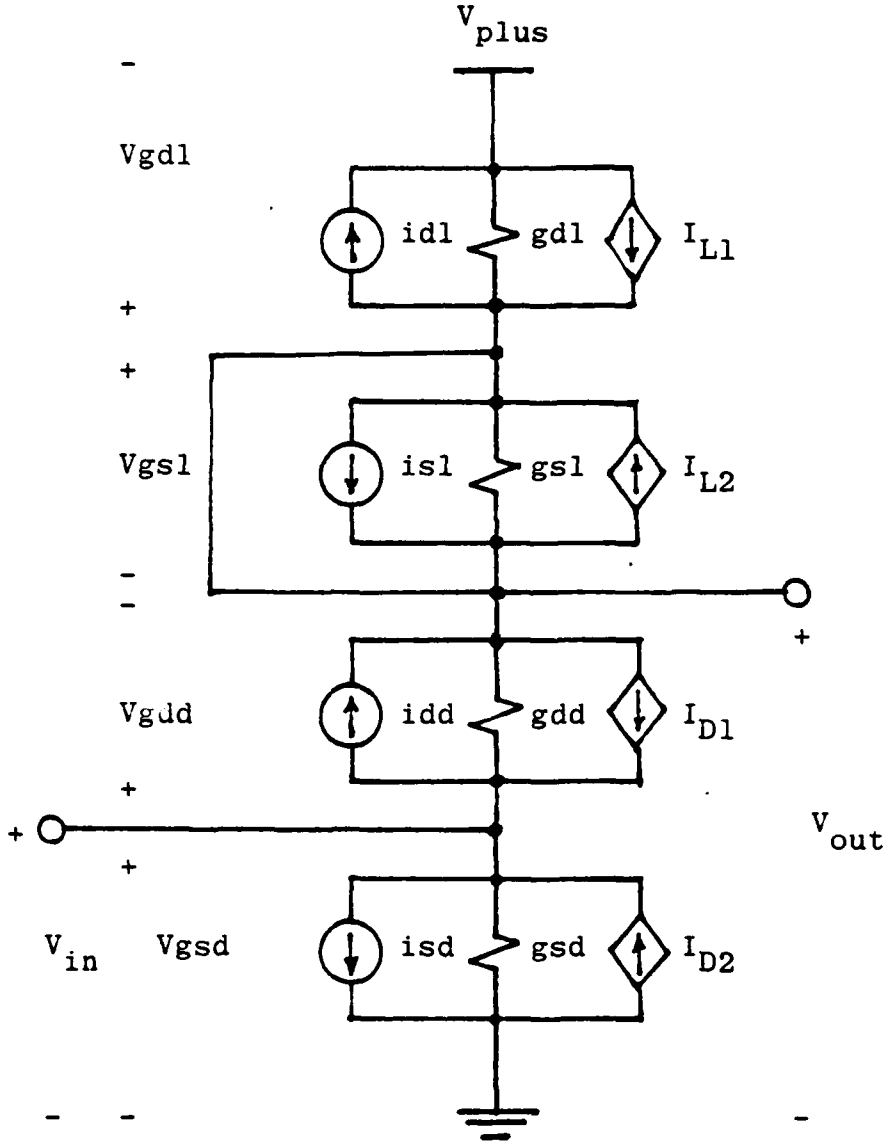
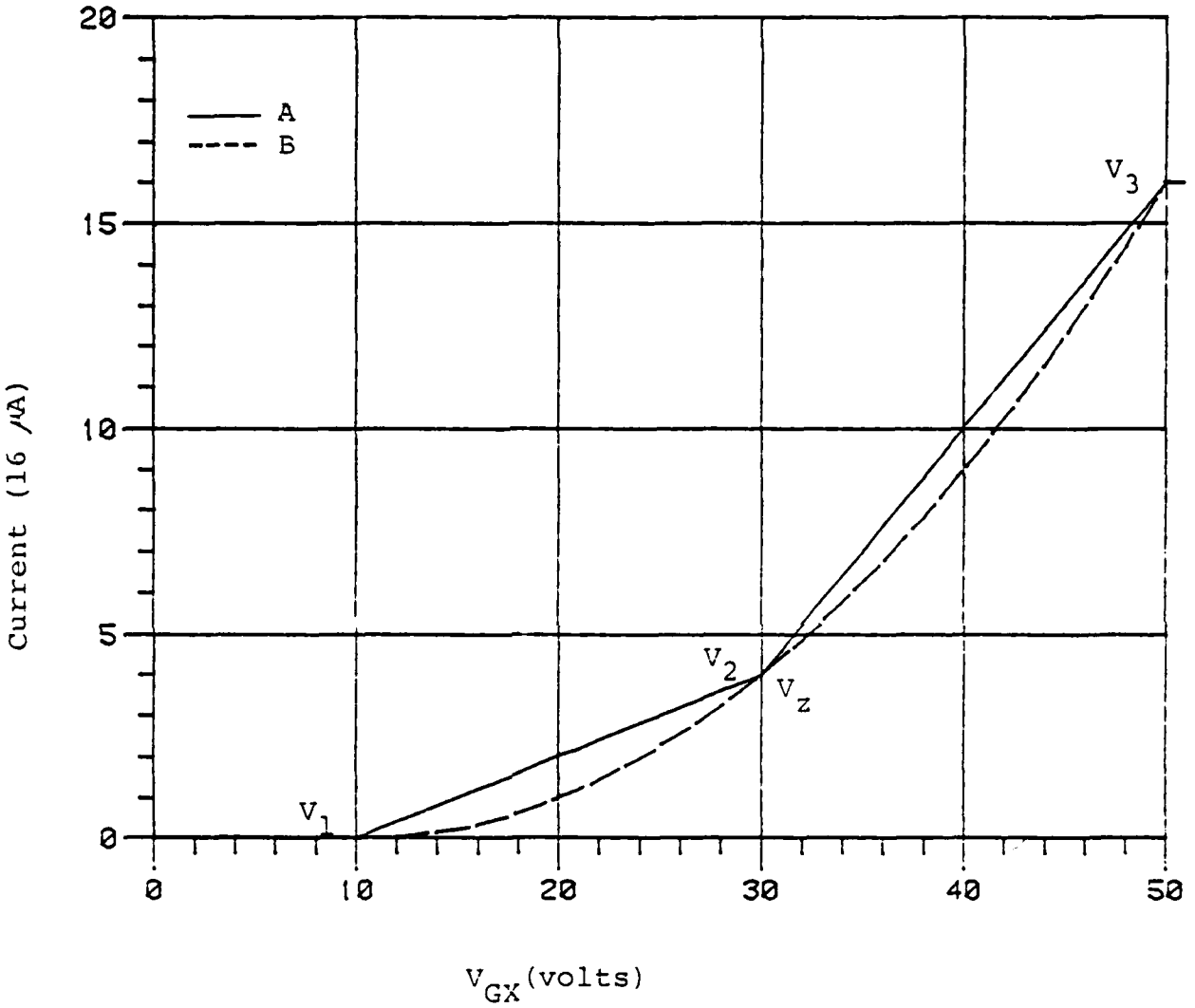


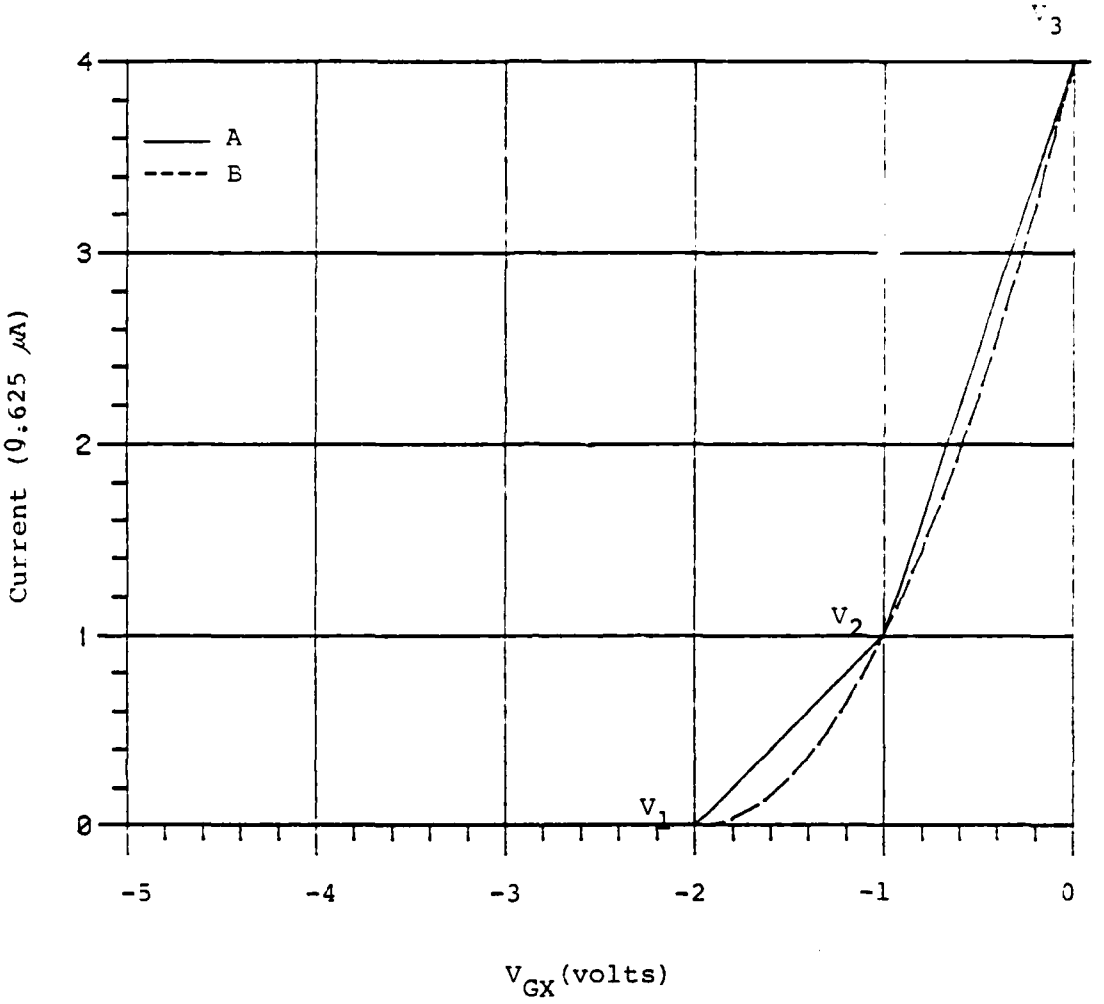
Fig. 3.2. PWL model for the inverter.



A = PWL segments

B = Actual i-v curve

Fig. 3.3a. PWL approximation by chord for the driver transistor



A = PWL segments

B = Actual i-v curve

Fig. 3.3b. PWL approximation by chord for the Depletion transistor.

Table 3.1a

Parameters of the Driver Transistor's i-v Curve by Chord Approximation

k	m_k(mhos)	j_k(A)	a_k(V)	b_k(V)
1	0	0	-5	V_{TD}
2	$K_D(V_z-V_{TD})$	$-K_D(V_z-V_{TD})V_{TD}$	V_{TD}	V_z
3	$K_D(V_{plus}+V_z-2V_{TD})$	$K_D(V_{TD}^2-V_{plus}*V_z)$	V_z	V_{plus}

Table 3.1b

Parameters of The Load Transistor's i-v Curve by Chord Approximation

k	m_k(mhos)	j_k(A)	a_k(V)	b_k(V)
1	0	0	-5	V_{TL}
2	$-0.5K_L*V_{TL}$	$0.5K_L*V_{TL}^2$	V_{TL}	$0.5V_{TL}$
3	$-1.5K_L*V_{TL}$	$K_L*V_{TL}^2$	$0.5V_{TL}$	0

terminal is given by

$$V_{out} = \frac{I_{LI}-I_{DI}+idd-idl+V_{in}*gdd+V_{plus}*gdl}{gdd+gdl} \qquad (3\text{-}1)$$

$$I_{LI} = Vgsl*gsl+isl \qquad (3\text{-}2a)$$

$$I_{DI} = Vgsd*gsd+isd \qquad (3\text{-}2b)$$

In the Katzenelson algorithm, gsd and isd are kept constant by the constant input, while gsl and isl are fixed by the zero gate-to-source potential at the load. However, gdl and gdd will vary across regions during the iterative process. Let $V_{out}^{(0)}$ be the initial guess of the output. Let $g_j^{(k)}$ and $i_j^{(k)}$ correspond to the parameters of segment j at the k^{th} iteration. Let $V_{out}^{(1)}$ be the first iterated solution. A solid logic 0 of 0.2 V has been preset as the initial guess at the output terminal regardless of the input.

Because of the initial guess, the $gdd_k^{(1)}$ always start in the same region as $gsd_k^{(1)}$ regardless of the input. The equality of these two resistors eliminates the terms that are associated with gdd, gsd, idd, and isd from Eq. (3-1). The initial guess also puts gdl and idl always in region 1 with zero values. For $V_{in} < 2.25$ V, the output V_{out} will vary across at least one breakpoint from the initial guess to the final value. The next breakpoint for gdl and gdd with the rising V_{out} is at $V_{plus}+V_{TL}$(3 V)and $V_{in}-V_{TD}(\leq 1.25$ V) respectively. Obviously, gdd will switch regions before gdl does. In this case, the small values of $idl_1^{(1)}$ and $gdl_1^{(1)}$ can be neglected from Eq. (3-1). The $V_{out}^{(1)}$ is simplified

in the following expression.

$$V_{out}^{(1)} = \frac{isl_3}{gdd_k^{(1)}} \qquad (3\text{-}3)$$

In the case where $V_{in} \leq V_{TD}$, $gdd_k^{(1)}$ is in region 1 with the zero value. Since isl_3 does not have a zero value, $gdd_1^{(1)}$ being zero puts $\hat{V}_{out}^{(1)}$ across the adjacent region.

In the case where 2.25 V > V_{in} > V_{TD}, $gdd_k^{(1)}$ is in region 2. From Table 3.1, Eq. (3-3) is given by

$$\hat{V}_{out}^{(1)} = \frac{k_L(-V_{TL})^2}{k_D(V_z-V_{TD})} = \frac{1.5625\ V^2}{V_z-1\ V} \qquad (3\text{-}4)$$

The condition for $\hat{V}_{out}^{(1)}$ to be able to travel to the next breakpoint is being larger than $V_{in}-V_{TD}(\leq 1.25\ V)$. Otherwise, $\hat{V}_{out}^{(1)}$ will remain in the same region as $V_{out}^{(0)}$ and iteration will be terminated with an incorrect solution. The above condition defines the requirement for V_z as follows:

$$V_z \leq \frac{\frac{k_L}{k_D}(-V_{TL})^2}{V_{in}-V_{TD}} = \frac{1.5626\ V^2}{V_{in}-1\ V} + 1\ V \qquad (3\text{-}5)$$

After V_z satisfied the requirement, the accuracy of the DC operating point will be evaluated for V_{in} < 2.25 V. At the operating point, V_{out} should have a value larger than 2.25 V. The final value of V_{out} puts gdd and idd in region 1. The expression for V_{out} (final) is given by

$$V_{out}^{(final)} = V_{plus} + \frac{isl_3 + idl_k^{(final)}}{gdl_k^{(final)}} - \frac{gsd_j^{(final)} * (V_{in} - V_{TD})}{gdl_k^{(final)}} \quad (3\text{-}6)$$

In the case where $V_{in} < V_{TD}$, $gsd_j^{(final)}$ becomes $gsd_1^{(final)}$ which means the term associated with $gsd_j^{(final)}$ can be neglected in Eq. (3-6). It is also reasonable to say $idl_k^{(final)}$ is in region 3 because of the small input. The resulting expression for $V_{out}^{(final)}$ is free of V_z.

$$V_{out}^{(final)} = V_{plus} = 5 \text{ V} \quad (3\text{-}7)$$

In the case where $gsd_j^{(final)}$ in region 2 ($2.25 \text{ V} > V_{in} > V_{TD}$), $gdl_k^{(final)}$ and $idl_k^{(final)}$ are in region 3 ($V_{out}^{(final)} \geq 4$ V), the following expression for $V_{out}^{(final)}$ is obtained.

$$V_{out}^{(final)} = V_{plus} - \frac{2 * k_D * (V_z - V_{TD}) * (V_{in} - V_{TD})}{k_L * (V_{TL})}$$

$$= 5 \text{ V} - \frac{2.56}{3} * (V_z - 1 \text{ V}) \quad (3\text{-}8)$$

In the case where $gsd_j^{(final)}$ is in region 2, $gdl_k^{(final)}$ and $idl_k^{(final)}$ are in region 2 ($3 \text{ V} \leq V_{out}^{(final)} \leq 4.0 \text{ V}$), the following expression for $V_{out}^{(final)}$ is obtained.

$$V_{out}^{(final)} = V_{plus} - \frac{2 * k_D (V_z - V_{TD}) * (V_{in} - V_{TD})}{k_L * V_{TL}} - V_{TL} \quad (3\text{-}9)$$

$$= 7 \text{ V} - 2.56 * (V_z - 1 \text{ V})$$

Equation (3-8) and Eq. (3-9) indicate $V_{out}^{(final)}$ is dependent on the breakpoint V_z. Table 3.2 illustrates the result of V_{out} by Katzenelson's algorithm with various values of V_z. It is easy to visualize the accuracy in degrading as V_z is placed farther and farther from the input.

On the segment approximation, the breakpoints give the exact value on the curve. The error is increasing away from the breakpoints to the mid-point of each segment. For the quadratic function

$$\hat{y} = (x - V_T)^2$$

it is possible to verify that the maximum errors occur at the midpoint of each segment as follows.

Let y be defined as Eq. (2-11) with (m_j, k_j, a_j, b_j).

At $x = a_j$ $\quad y = y_a = (a_j - V_T)^2$ (3-11a)

At $x = b_j$ $\quad y = y_b = (b_j - V_T)^2$ (3-11b)

$$m_j = \frac{y_b - y_a}{b_j - a_j} \equiv (a_j + b_j) - 2V_T \qquad (3\text{-}11c)$$

Let error e be

$$e = \hat{y} - y = (x - V_T)^2 - (m_j x + k_j) \qquad (3\text{-}12a)$$

$$\frac{de}{dx} = 2(x - V_T) - m_j \qquad (3\text{-}13)$$

Setting de/dx to zero gives

$$x = \frac{m_j}{2} + V_T \qquad (3\text{-}14a)$$

Table 3.2

Inverter DC Output With "Chord" Approximation

V_z(V)	$\hat{V}_o^{(1)*}$(V)	$V_{out}^{(final)}$(V)
2.0	1.56	4.15
2.1	1.42	4.06
2.2	1.30	3.93
2.3	1.20	3.67
2.4	1.12	3.42
2.5	1.04	3.16
2.5625	1.00	3.00
2.6	0.927	0.927
2.7	0.919	0.919
2.8	0.868	0.868
2.9	0.822	0.822
3.0	0.781	0.781

V_{in} = 2.0 V

$V_{out}^{(final)}$ = 4.2 V by "functional" model

*It is necessary for $\hat{V}_o^{(1)} \geq V_{in}-V_{TD}$ for the trajectory to cross into other regions.

From Eq. (3-11c),

$$x = \frac{a_j+b_j}{2} \qquad (3\text{-}14b)$$

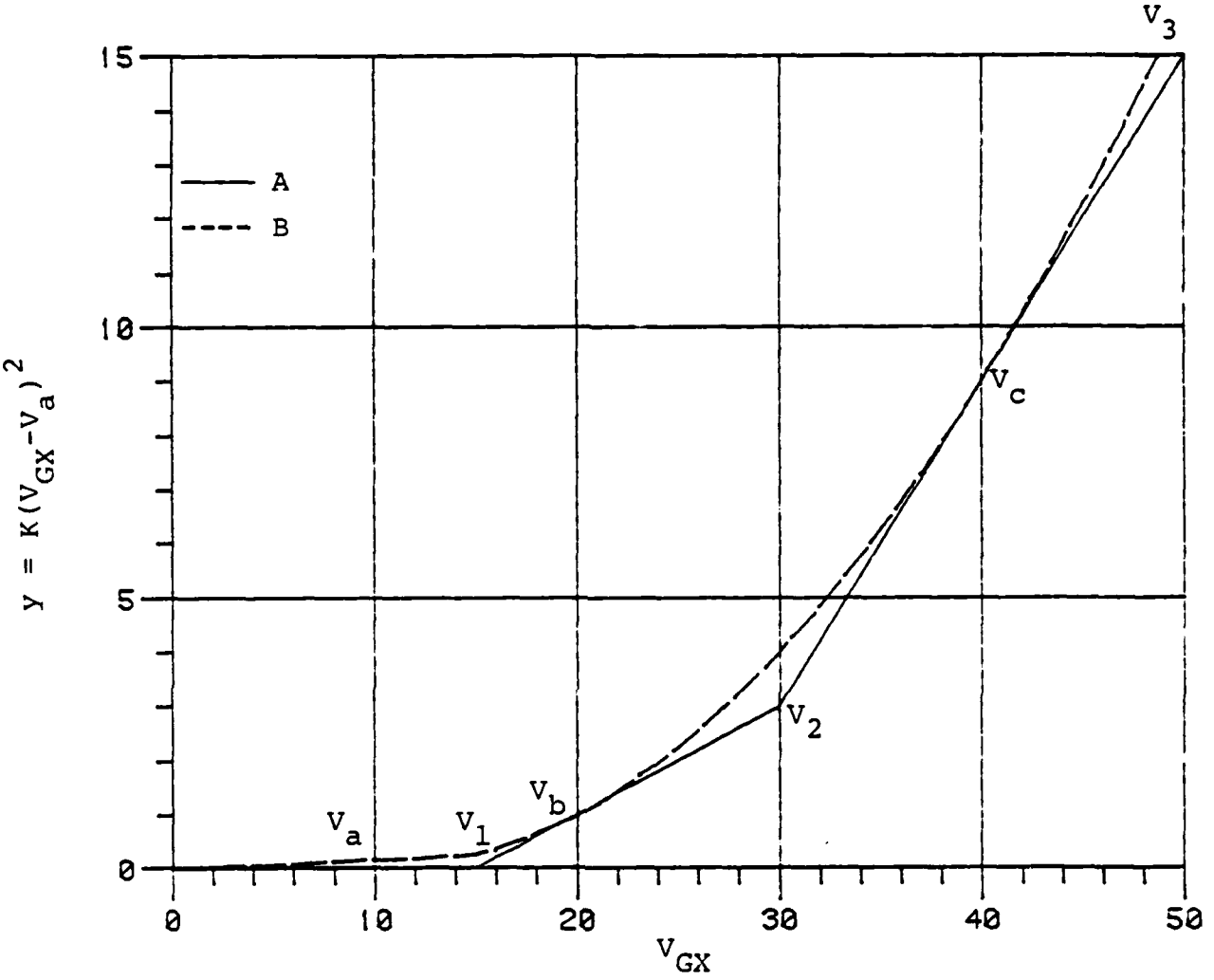
The maximum error at segment 2 is as high as 100% regardless of how many segments are used. The higher values of V_z in Table 3.2 have the effect of putting V_{in} (2 V) closer to maximum error point. Therefore, the selection of V_z is considered as crucial in the approximation method by the chord.

3.3 Approximation by Tangent

An alternative way of approximating functions by PWL segments is to use tangent rather than the chord. The i-v curve of a nonlinear resistor is shown in Fig. 3.4 with the new 3-segment representation. The procedure for choosing the PWL segments is as follows. First, the voltage axis is divided up into intervals. Instead of connecting the endpoints of these intervals to form the slope of segments, the slope is taken as the slope of the tangent at these points. The slope at each end point is represented by its tangent line which defines a particular segment for the new intervals. Then the intersections of these tangent lines define a new set of breakpoints. Again, the necessary parameters for the segments are tabulated. The relationships among the tangent points and the breakpoints will be analyzed.

Let V_a,V_b, and V_c be the chosen tangent points as shown in Fig. 3.4. For

$$i = K(V_{GX}-V_T)^2 \qquad V_T \leq V_{GX} \leq V_{end} \qquad (3\text{-}15)$$



A = PWL segments

B = Actual i-v curve

Fig. 3.4 PWL approximation by tangent.

the slope of the tangent line at V_u is

$$\left.\frac{di}{dV_{GX}}\right|_{V_u} = 2K(V_u - V_T) \tag{3-16}$$

The slopes of the tangent line at V_a, V_b, and V_c are shown in column 2 of Table 3.3. A zero value of conductance is used to represent the horizontal tangent line at V_a. The current intercept of the segment containing tangent point V_u is

$$k_j = K(V_T^2 - V_u^2) \tag{3-17}$$

The relationships among the breakpoints and tangents are obtained as follows. Let segment j contain the tangent point V_a, and segment j+1 contain the tangent point V_b. The intersection of these two tangent lines gives the new breakpoint.

$$m_j x + k_j = m_{j+1} x + k_{j+1} \tag{3-18}$$

where m_j, m_{j+1}, k_j and k_{j+1} are defined as Eq. (3-16) and Eq. (3-17). Solving Eq. (3-18) gives the following

$$\begin{aligned} x &= \frac{k_j - k_{j+1}}{m_{j+1} - m_j} \\ &= \frac{k[(V_T^2 - V_a^2) - (V_T^2 - V_b^2)]}{2k[(V_b - V_T) - (V_a - V_T)]} \\ &= \frac{V_a + V_b}{2} \end{aligned} \tag{3-19}$$

The breakpoints in terms of tangent points are given by the following:

$$V_1 = \frac{V_T+V_b}{2} \tag{3-20a}$$

$$V_2 = \frac{V_b+V_c}{2} \tag{3-20b}$$

$$V_3 = V_{end} \tag{3-20c}$$

It is noted that the maximum error occurs at the breakpoints as shown in Fig. 3.4 and their relationships to the tangent points are as follows:

$$e_1 = \frac{K}{4} (V_b-V_T)^2 \tag{3-21a}$$

$$e_2 = \frac{K}{4} (V_c-V_b)^2 \tag{3-21b}$$

$$e_3 = K (V_{end}-V_c)^2 \tag{3-21c}$$

If the maximum error is too big,then additional tangent lines can be added at the breakpoint where the maximum error occurs to reduce the error.

The input-output characteristics of the inverter will be used again to investigate the accuracy of the approximation. The selection of the tangent point V_a is necessary to be $V_a \leq V_T$; otherwise, more than three segments will be established. The selection of the tangent point V_b is very critical because the breakpoint V_1 or the effective threshold voltage is determined by its value. Although the maximum error e_1 is also determined by V_b, the effect on the DC operation is not significant. However, any discrepancy of the threshold voltage in timing analysis will contribute to major errors. Hence, it

is desired to put V_b as close as possible to V_T without causing an unacceptable trade-off in the maximum error e_2. V_c is selected as a compromise to reduce both e_2 and e_3. The above criterion of selecting tangent points is applicable to both the enhancement and depletion transistors. The associated parameters are entered in Table 3.3 in terms of the tangent points.

Table 3.3

Associated Parameters for The Segments by "Tangent" Approximation

k	m_k(mhos)	j_k(A)	a_k(V)	b_k(V)
1	0	0	$-V_{plus}$	$0.5(V_T+V_b)$
2	$2K(V_b-V_T)$	$K(V_T^2-V_b^2)$	$0.5(V_T+V_b)$	$0.5(V_c+V_b)$
3	$2K(V_c-V_T)$	$K(V_T^2-V_c^2)$	$0.5(V_c+V_b)$	V_{end}

Accuracy measurements are emphasized on the approximation of the driver because of its longer active region. An arbitrary set of tangent points based on the above criterion is selected for the depletion load. Results of various sets of tangent points with input V_{in} set at maximum error points are compared with the result by the "functional" model in Table 3.4. This method of segment approximation provides accurate DC analysis and resolves the major problems of the chord approximation method.

Table 3.4

Inverter DC Output With "Tangent" Approximation

V_a (V)	V_b	V_c	V_1 (V)	V_2	V_3	$V_{out}(V_{in} = V_1)$ (V)		$V_{out}(V_{in} = V_2)$ (V)		$V_{out}(V_{in} = V_3)$ (V)	
						PWL model	Functional model	PWL model	Functional model	PWL model	Functional model
1.00	2.00	4.00	1.50	3.00	5.00	5.00	4.83	0.735	0.439	0.260	0.20
1.00	2.00	3.50	1.50	2.75	5.00	5.00	4.83	0.735	0.525	0.313	0.20
1.00	2.25	4.00	1.63	3.13	5.00	5.00	4.73	0.586	0.407	0.260	0.20
1.00	2.25	3.75	1.63	3.00	5.00	5.00	4.73	0.586	0.439	0.284	0.20
1.00	2.50	4.00	1.75	3.25	5.00	5.00	4.60	0.488	0.379	0.260	0.20
1.00	2.50	3.50	1.75	3.00	5.00	5.00	4.60	0.488	0.439	0.313	0.20

Tangent set for the depletion load is (-2, -1, -0.25).

Chapter 4

MODEL VALIDATION

4.1 Introduction

Although acceptable DC results are achieved in the inverter circuit, more detailed study is needed to understand the effect of the PWL approximation on the accuracy of the transient response. For an understanding of the transient behavior of the network model, the circuit shown in Fig. 4.1 will be analyzed. In addition, the PWL model will be used to construct a multiple-input gate. The 2-input NAND gate shown in Fig. 4.2 is chosen to study the effect of the floating node as a consequence of stacking MOS transistors [11].

To simplify the analysis, the following assumptions will be used throughout the thesis:

> Assumption: All output capacitances are combined into a simple equivalent load capacitance (C_L). This simplification allows an analytical solution to be developed which is adequate for most MOS transient design problems.

Initially, the voltage input to the inverter will be a step function for both the turn-off and turn-on cases. The first case is assumed to have a value V_{in} = 0.2 V, and the second case to have a value of V_{in} = 5 V.

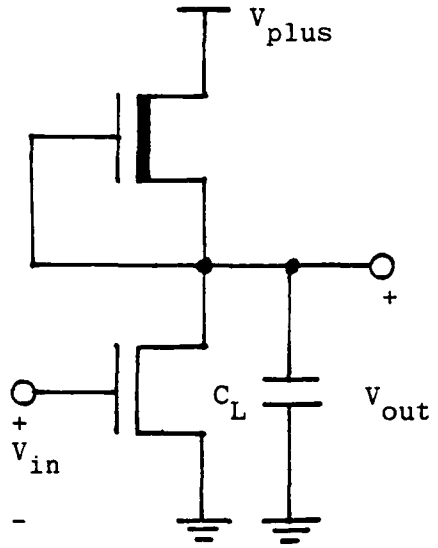


Fig. 4.1. Inverter gate.

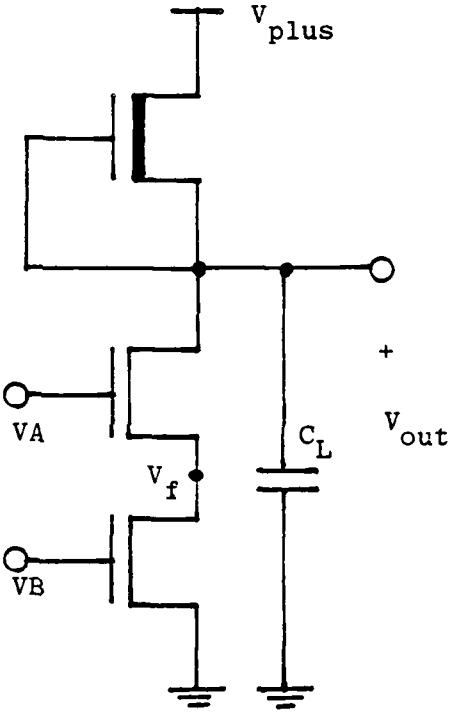


Fig. 4.2. 2-input NAND gate.

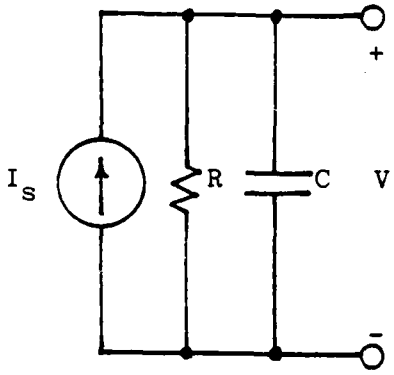


Fig. 4.3. First-order dynamic network.

4.2 Piecewise-Linear Approach

One of the most basic problems in nonlinear dynamic network analysis is to solve the nonlinear differential equations. Most of this tedious process can be eliminated by the PWL approach. One way of analyzing a first-order dynamic network is to obtain the equation of motion in the normal form in terms of the state variable V_c of the capacitor and solve it.

Because of the PWL characterization of the network model, it is possible to construct at any time $t = t_o$ a network which consists only of linear resistors and capacitors since at any given time a PWL network must operate on some linear segment k. The response will continue to stay in the same segment k until it reaches one of the breakpoints of this segment at some time $t = t_1$. During the time interval (t_o, t_1) the nonlinear resistance appears linear to the energy-storage element (capacitor). Therefore, it can be replaced by its Thevenin or Norton equivalent circuit. The resulting network conceptually is the simplest 1^{st} order dynamic network which has the general form of Fig. 4.3. The corresponding normal-form equation is given by

$$C \frac{dV}{dt} + \frac{V}{R} = I_s \qquad (4\text{-}1)$$

Solving the differential equation gives the following familiar expression,

$$V(t) = V_k(t_e) + [V_k(t_o) - V_k(t_e)] e^{-(t-t_o)/\tau_k} \qquad t \geq t_o \quad (4\text{-}2a)$$

where $V_k(t_o)$ is the initial state at segment k

$V_k(t_e)$ is the equilibrium state at segment k

τ_k is the time constant at segment k

In the case where the PWL segment k in the i-v characteristics is horizontal or $R \to \infty$, solving Eq. (4-1) gives the following linear expression:

$$V(t) = V_k(t_o) + \frac{I_s}{C}(t-t_o) \qquad (4\text{-}2b)$$

If the above interpretation for V(t) is applied to all times $t \geq t_o$, the resulting curve will define the trajectory. The trajectory always starts from the initial state corresponding to $t=t_o$. Since the motion of the network is completely described by its trajectory starting from the prescribed initial state, the pertinent segment k containing the initial state will be used to determine the equilibrium state and the time constant corresponding to segment k. An examination of Eq. (4-2) shows that it is completely specified by the three parameters, namely, the $V_k(t_o)$, $V_k(t_e)$, and τ_k. Given these three parameters, the solution V(t) can be obtained by inspection without having to solve the associated differential equation. This observation is the key to the table lookup method that we are going to apply.

It is noted that Eq. (4-2a) is valid only for all time $t \geq t_o$ for which the value V(t) falls within the interval of definition of segment k and V(t) eventually will settle down asymptotically to the equilibrium state for all time $t \geq t_o$.

If the value of $V_k(t_e)$ is within the interval of definition of segment k for all times $t \geq t_o$, then the complete solution consists of the single exponential time function. If the value of $V_k(t_e)$ exceeds the interval of definition of segment k, then the time $t = t_1$ where v(t) reaches the breakpoint of segment k must be determined. The exponential solution is then valid only for $t_o \leq t \leq t_1$. From Eq. (4-2a), the time t_1 can be found easily from the following equation

$$t_1 = \tau_k \ln \frac{V_k(t_1) - V_k(t_e)}{V_k(t_o) - V_k(t_e)} + t_o \qquad (4\text{-}3)$$

At $t = t_1$, $V(t_1)$ is chosen as the new initial state. The parameters will be evaluated at this breakpoint within the new segment and the process is repeated as many times as necessary until the solution V(t) reaches the final specified time t_f. Remark: The DC solution at $t = 0^-$ is used as the first initial state.

4.2.1 Inverter circuit

The network model of the inverter is shown in Fig. 4.4. Taking KCL at the output terminal gives

$$C\frac{dV_o}{dt} + I_{D1} + idl + gdl*vgdl - I_{L1} - idd - Vgdd*gdd = 0 \qquad (4\text{-}4)$$

where $I_{D1} = Vgsd*gsd + isd$

$I_{L1} = Vgsl*gsl + isl$

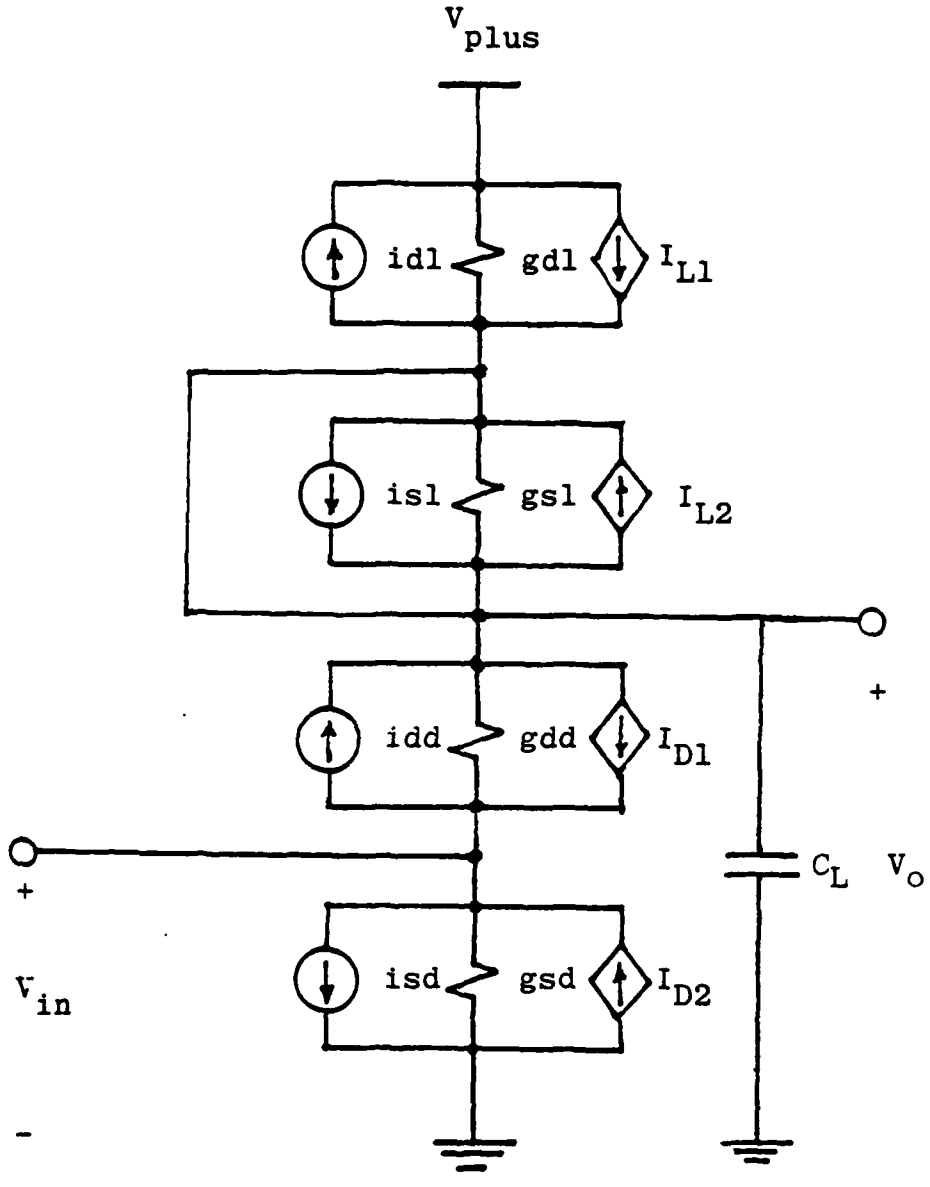


Fig. 4.4. PWL model of Fig. 4.1.

$$V_{gsd} = V_{in}$$

$$Vgdd = V_{in} - V_o$$

$$Vgsl = 0$$

$$Vgdl = V_o - V_{plus}$$

Rearrangement of Eq. (4-4) gives the Norton equivalent form of Eq. (4-1) with the following values for the elements

$$R = \frac{1}{gdd+gdl} \tag{4-5}$$

$$I_s = K_1 + K_2 * V_{in} \tag{4-6}$$

where $K_1 = (idd-isd) + (isl-idl) + V_{plus}*gdl$

$K_2 = gdd - gsd$

In the turn-off case, the zero value of the input causes all the model parameters of the driver to be small which could then be neglected in Eq. (4-4). In this case, Eq. (4-4) is governed by the i-v characteristics of the depletion load. Various sets of tangent points for the approximation of the i-v curve on the load have been used to observe the output risetime. Numerical results using the PWL approach are compared with those of SPICE2. Although all the results are close to those of SPICE2, the possible accumulative error on the delay time when a series of inverters are connected is investigated. The set of (-2 V, -1.5 V, -0.5 V) was found to cause the smallest error in the delay time and thus will be used throughout the remainder of this thesis. A similar

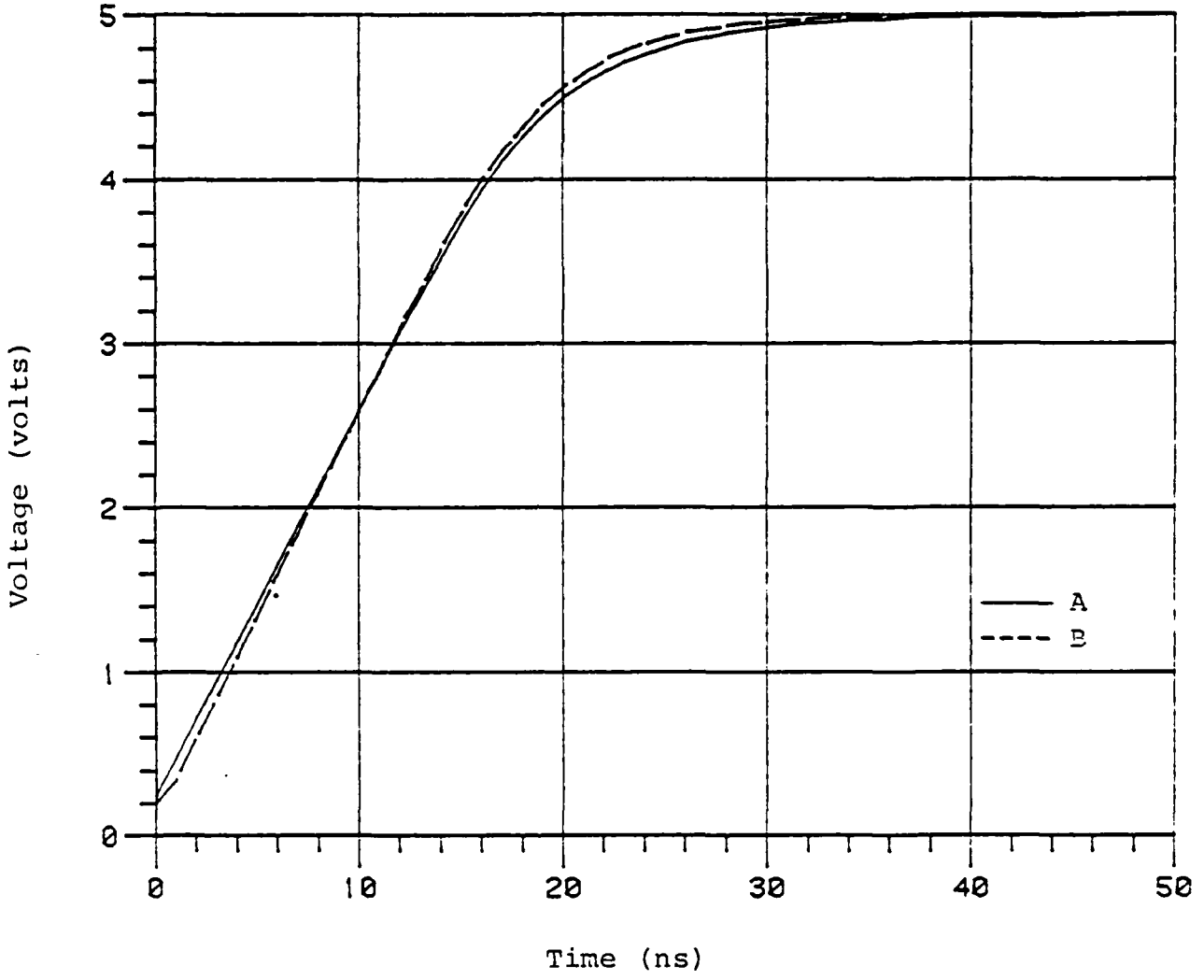
procedure is applied to the turn-on case to find a better set of tangent points for the i-v curve of the enhancement driver. Unlike the turn-off case, the depletion load does carry some impact on the zero-state response of the output. Since the W/L ratio of the driver is very much larger than the corresponding ratio for the load, the discharging current through the driver will be much larger than the charging current through the load. Hence, the output is more dependent on the discharging current. Initially, when V_{out} is high, the driver is in the saturation region which carries a large discharging current. However, the variation on the threshold voltage due to the PWL approximation effectively lengthens the saturation region of the driver. As a consequence, the driver stays longer in saturation and produces more discharging current at the beginning time. As a result of the larger discharging current, the fall time by this model is shorter than the SPICE2 output. However, the responses should be adequate for most practical circuit design. The results with the chosen sets of tangent points for both cases are shown in Fig. 4.5.

4.2.2 NAND Circuit

The device symbol for a 2-input NAND is shown in Fig. 4.2 and the PWL model of the device is shown in Fig. 4.6. Taking KCL at the output terminal gives

$$I_{L1}+idd_1+Vgdd_1*gdd_1 = I_{D1}+Vgd1*gd1+id1+C\frac{dV_o}{dt} \qquad (4\text{-}7)$$

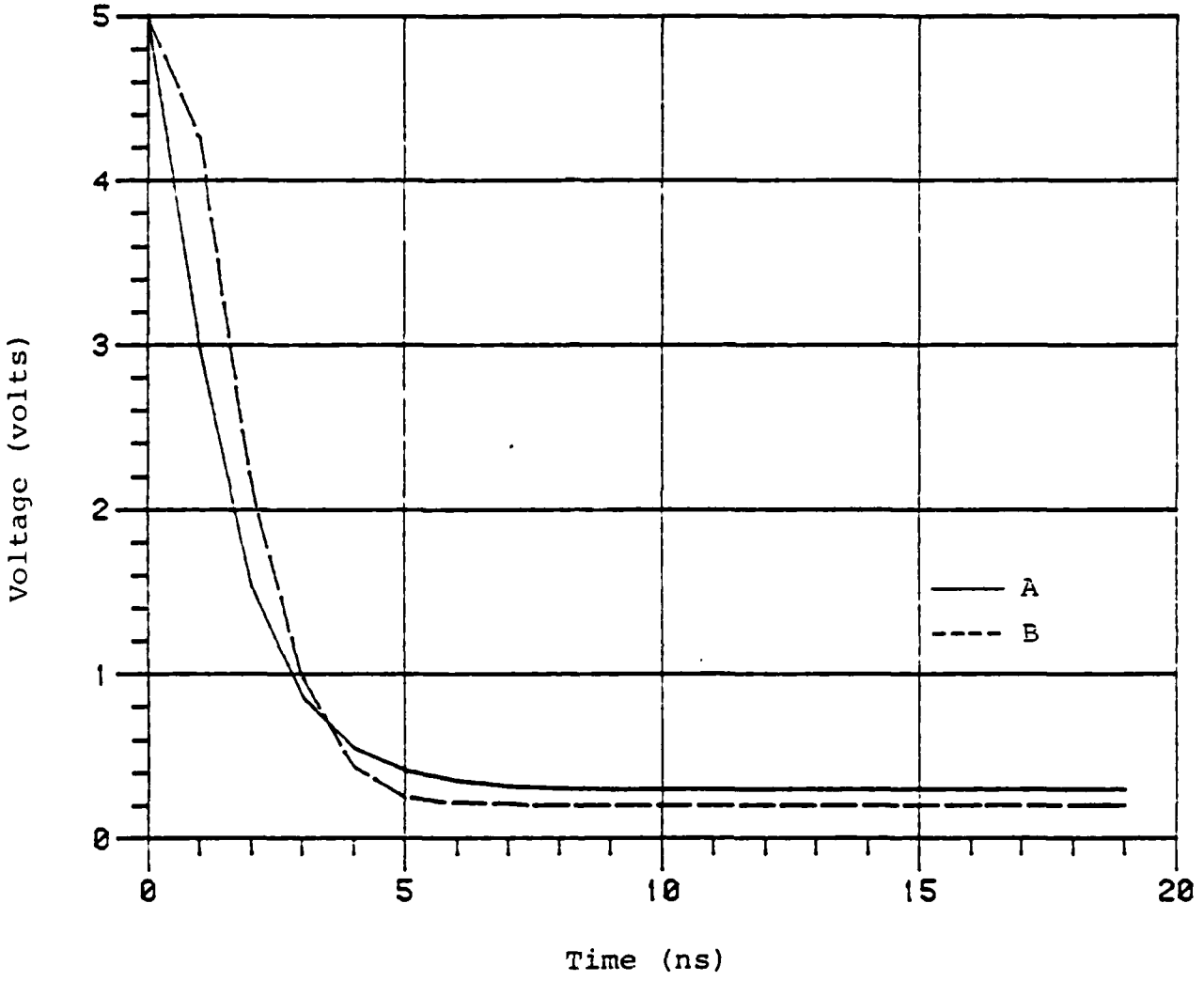
where I_{L1} = Vgs1*gs1 + is1



A = PWL model with step input

B = SPICE2 output

Fig. 4.5a. Turn-off case for the inverter.



A = PWL model with step input

B = SPICE2 output

Fig. 4.5b. Turn-on case for the inverter.

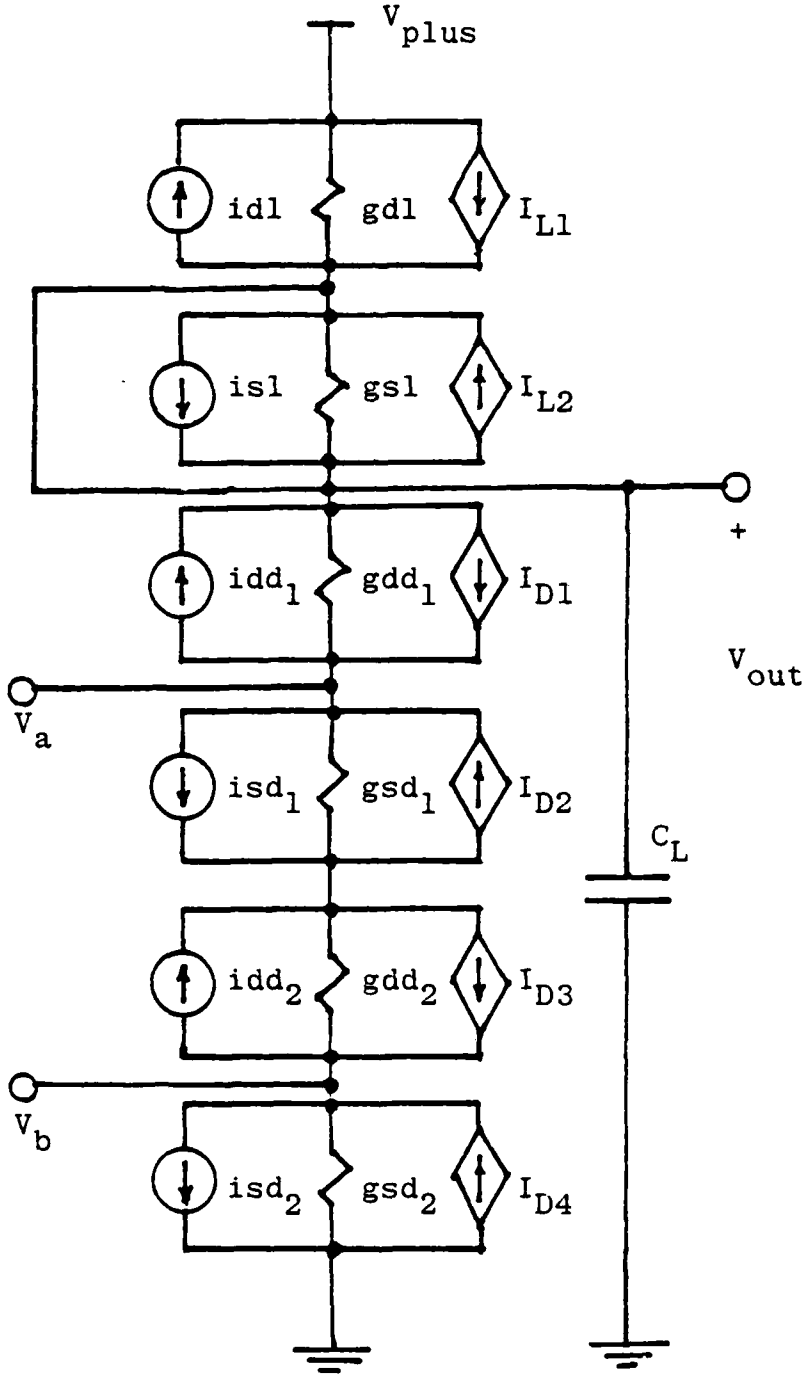


Fig. 4.6. PWL model for Fig. 4.2.

$$I_{D1} = Vgsd_1 * gsd_1 + isd_1$$

$$Vgdd_1 = V_a - V_o$$

$$Vgdl = V_o - V_{plus}$$

$$Vgsd_1 = V_a - V_f$$

$$Vgsl = 0$$

Taking KCL at the floating mode V_f gives

$$I_{D2} + I_{D3} = Vgsd_1 * gsd_1 + isd_1 + Vgdd_2 * gdd_2 + idd_2 \qquad (4\text{-}8)$$

where $I_{D2} = Vgdd_1 * gdd_1 + idd_1$

$$I_{D3} = Vgsd_2 * gsd_2 + isd_2$$

$$Vgsd_1 = V_a - V_f$$

$$Vgdd_2 = V_b - V_f$$

$$Vgdd_1 = V_a - V_o$$

$$Vgsd_2 = 0$$

DC analysis by Katzenelson's algorithm is performed by taking V_f as an unknown variable and setting dV_o/dt to zero. Equation (4-7) and Eq. (4-8) are put in the following forms to find the DC operating point.

$$\begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} V_o \\ V_f \end{bmatrix} = \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \qquad (4\text{-}9)$$

where $g_{11} = gdd_1 + gdl$

$$g_{12} = -gsdl$$

$$g_{21} = -gdd_1$$

$$g_{22} = gsd_1 + gdd_2$$

$$I_1 = isl-idl+idd_1-isd_1+V_a(gdd_1-gsd_1)+V_{plus}*gdl$$

$$I_2 = isd_1-idd_1+idd_2-isd_2+V_a(gsd_1-gdd_1)+V_b(gdd_2-gsd_2)$$

Due to the nature of the logic function of the NAND gate, an initial guess of 5 V is set to the output and the floating node for faster convergence. DC analysis with 4 possible combinations of inputs is illustrated in Table 4.1.

Table 4.1

DC Logic Function of 2-input NAND

V_a	V_b	V_o	V_f
0.25 V	5.0 V	5.0 V	0.0 V
0.25 V	0.25 V	5.0 V	2.5 V
5.0 V	5.0 V	0.29 V	0.15 V
5.0 V	0.25 V	5.0 V	3.5 V

For the transient analysis, the relationship between V_o and V_f is derived from Eq. (4-8) and expressed as follows:

$$V_f = \frac{(V_o-V_x)*gdd_1}{gdd_2+gsd_1} \qquad (4\text{-}10)$$

where

$$V_x = \frac{V_a(gdd_1-gsd_1)+V_b(gsd_2-gdd_2)+(idd_1-isd_1)+(isd_2-idd_2)}{gdd_1}$$

Substituting Eq. (4-9) into Eq. (4-7) gives the Norton equivalent form of Eq. (4-1) with the following values for the elements:

$$R = \frac{1}{gdl+gdd_1 - \frac{gsd_1 gdd_1}{gdd_2+gsd_1}} \qquad (4\text{-}11)$$

$$I_s = K_1+K_2*V_a+K_3*V_b \qquad (4\text{-}12)$$

where

$$K_1 = (idd_1-isd_1)+(isl-idl)+V_{plus}*gdl+\frac{gsd_1}{gsd_1+gdd_2}$$

$$[(isd_1-idd_1)+(idd_2-isd_2)]$$

$$K_2 = \frac{gdd_2*(gdd_1-gsd_1)}{gsd_1+gdd_2}$$

$$K_3 = \frac{gsd_1*(gdd_2-gsd_2)}{gsd_1+gdd_2}$$

Results with all the 16 possible step inputs as shown in Table 4.2 are observed. After the adjustment of the W/L ratio on the load, the responses of the NAND gate are almost identical to that of the inverter. The cases for rising and falling responses are shown in Figs.4.7 (a) and (b), respectively.

Table 4.2

Possible Inputs for Transient Analysis

V_a		V_b		V_o
$t=0^-$	$t>0^+$	$t=0^-$	$t>0^+$	$t>0^+$
0	0	0	0	a
0	0	0	1	a
0	0	1	0	a
0	0	1	1	a
0	1	0	0	a
0	1	0	1	c
0	1	1	0	a
0	1	1	1	c
1	0	0	0	a
1	0	0	1	a
1	0	1	0	d
1	0	1	1	d
1	1	0	0	a
1	1	0	1	c
1	1	1	0	d
1	1	1	1	b

0 = 0.25 V

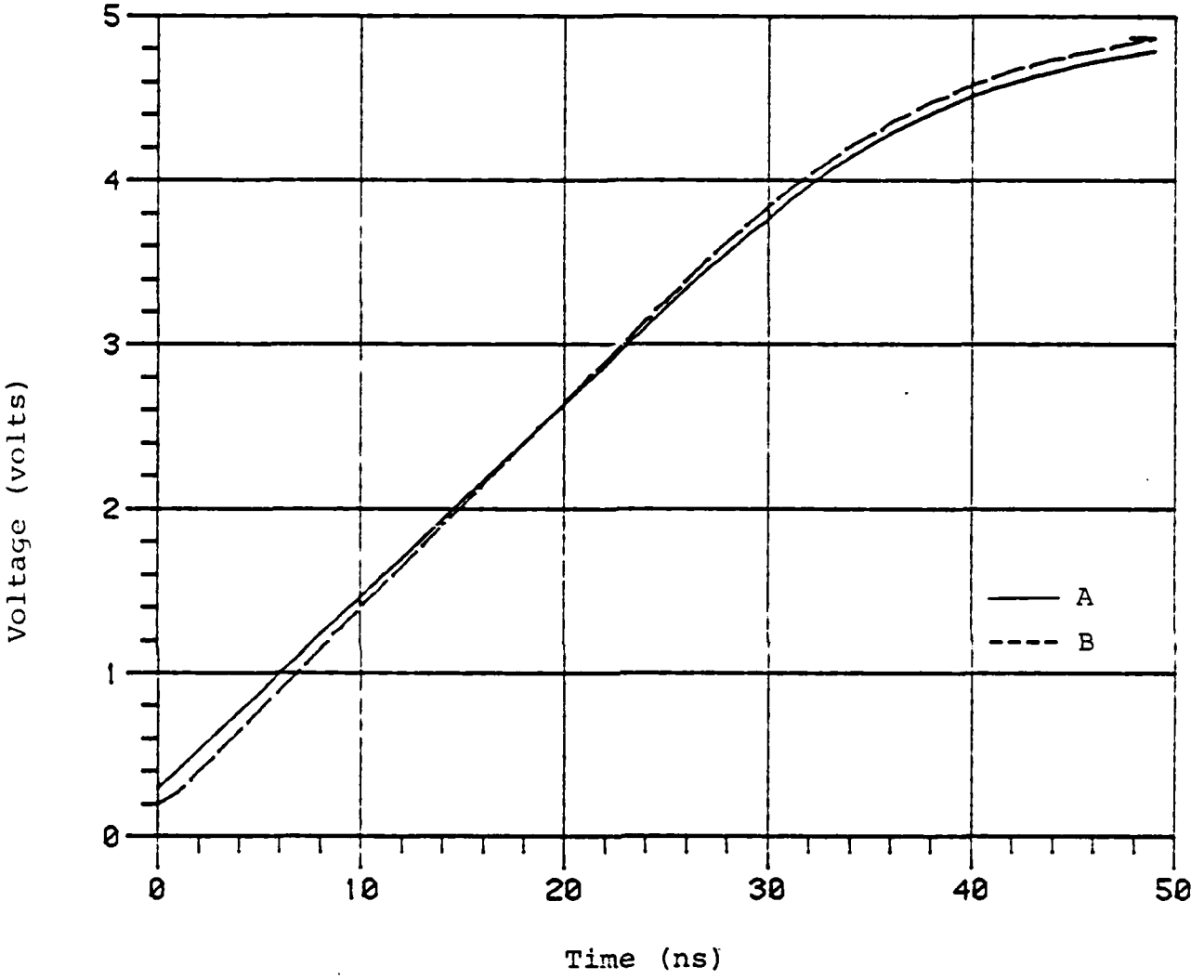
1 = 5.0 V

a - output stays high

b - output stays low

c - output goes from high to low

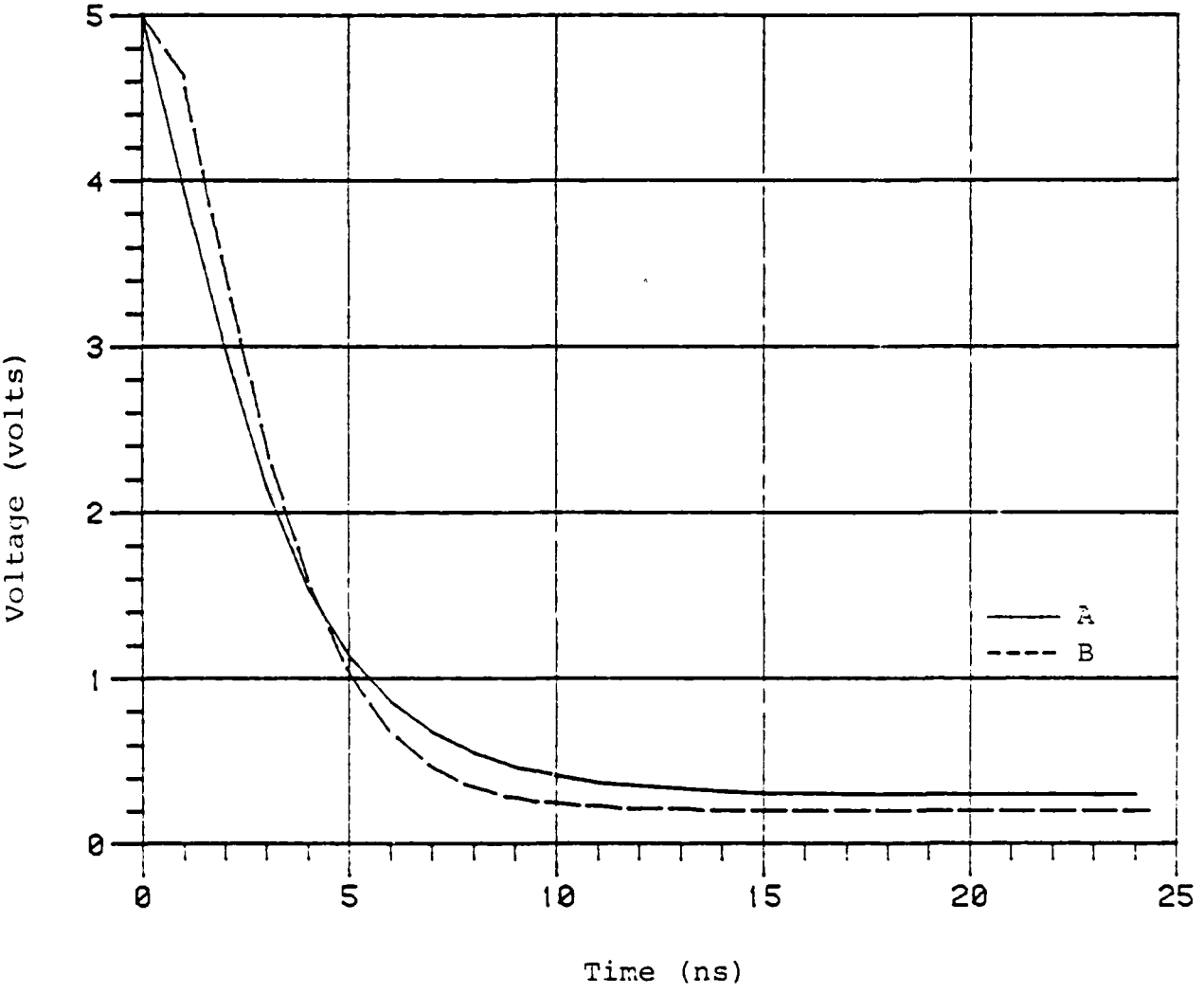
d - output goes from low to high



A = PWL model with step inputs

B = SPICE2 output

Fig. 4.7a. Turn-off case for the 2-input NAND gate.



A = PWL model with step inputs

B = SPICE2 output

Fig. 4.7b. Turn-on case for the 2-input NAND gate.

Chapter 5

WAVEFORM APPROXIMATION

5.1 Introduction

In general, the signals in a circuit are not step functions, and the techniques discussed in the previous section are not directly applicable. Solving the differential equation of Eq. (4-1) with exponential input, for example, gives a nonlinear transcendental equation of the general form,

$$Ae^{-a_1 t} + Be^{-a_2 t} = C \qquad (5\text{-}1)$$

Solving this equation for the variable t is a time-consuming task and often needs a number of iterations to find the point where the trajectory crosses a breakpoint. To simplify the task, two methods of approximating waveforms have been investigated: the first uses a discrete stepwise function approximation, and the second uses a PWL approximation. As shown in Chapter 4, the PWL approach with step input gives a simple output expression which can be determined by 3 pieces of information. The discrete stepwise function defines constant level of voltage at prescribed intervals. During each interval, the input can be treated as a step function which allows the analysis by the method described in Chapter 4. To test this approach, a step input is applied at the first stage of a chain of 10 inverters, and output of each stage is observed. The output waveform of each stage is approximated by

a stepwise function and fed into the next stage as an input.

In many cases, when there is feedback in a circuit system the system will not be unidirectional and the subcircuits within the feedback loop can no longer be analyzed as a sequence of stages without iteration. It will be computationally inefficient to consider the entire circuit as a big subcircuit. Hence, the Gauss-Seidel WR method will be employed to decompose the circuits into several dynamical subcircuits each of which is analyzed independently for the entire time interval [7]. A number of iterations are needed for the waveform to converge to the solution, provided it converges. A 3-inverter ring oscillator will be used to illustrate the application of WR technique to circuits with feedback.

Another fact which may cause computational problems in MOS digital circuit design is the presence of pass transistors. The pass transistor has a coupling effect when the device is turned on and both its drain and source are charging or discharging at the same time. A subcircuit which includes pass transistors results in 2 or more dimensional differential equations. The WR method will be used again to decompose the pass transistor into individual subcircuits. A simple network with pass transistor will be used as an example.

Although the WR method is found to be efficient, it does suffer from a convergence problem when strong feedback exists. Such a problem is demonstrated by the bootstrap circuit.

5.2 Discrete Stepwise Representation

An exponential function of V_{in} in Eq. (4-1) gives rise to nonlinear transcendental equations. To avoid solving these equations, a stepwise function is proposed to represent the exponential waveform. A stepwise function can be represented as

$$V_{in} = V_j \qquad \text{for } t_a \leq t \leq t_b \qquad (5\text{-}2)$$

Let V_j be the step level while t_a and t_b be the step sizes. During the interval (t_d, t_b), V_{in} is constant. Thus, the input can be treated as a step function and solved by the method described in Chapter 4.

A set of sampling points is chosen to set up the step representation. One way to choose the sampling points is to take the percentage of the difference between the maximum and minimum values of the waveform as specifications for the sampling points. The 10-stage inverter chain shown in Fig. 5.1 will be used as an example for the stepwise representation.

In the turn-off case where the input waveform is changing from high to low, the output is charging up from low to high mainly by the current through the load transistor. A low level of input can be reached abruptly because the input typically is decaying very fast. For the short full time of the input, we found that a 2-step representation as shown in Fig. 5.2a gives good accuracy.

In the turn-on case where the input waveform is from low to high, the output is discharging from high to low mainly by the current through the driver transistor. Because of the

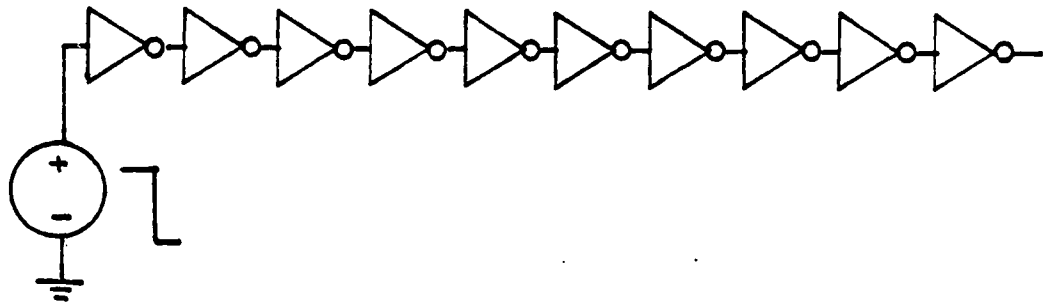
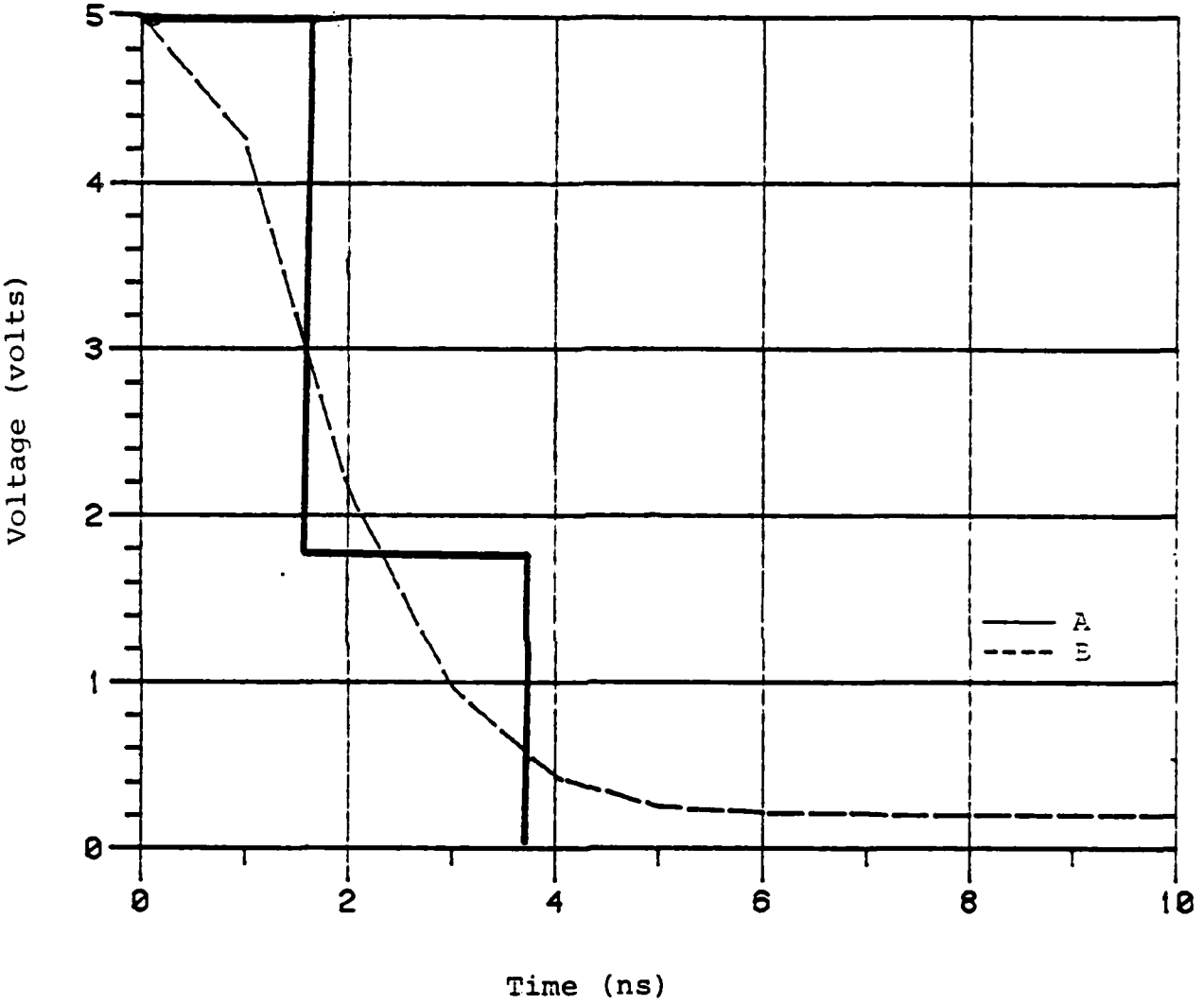


Fig. 5.1. Ten-stage inverter chain



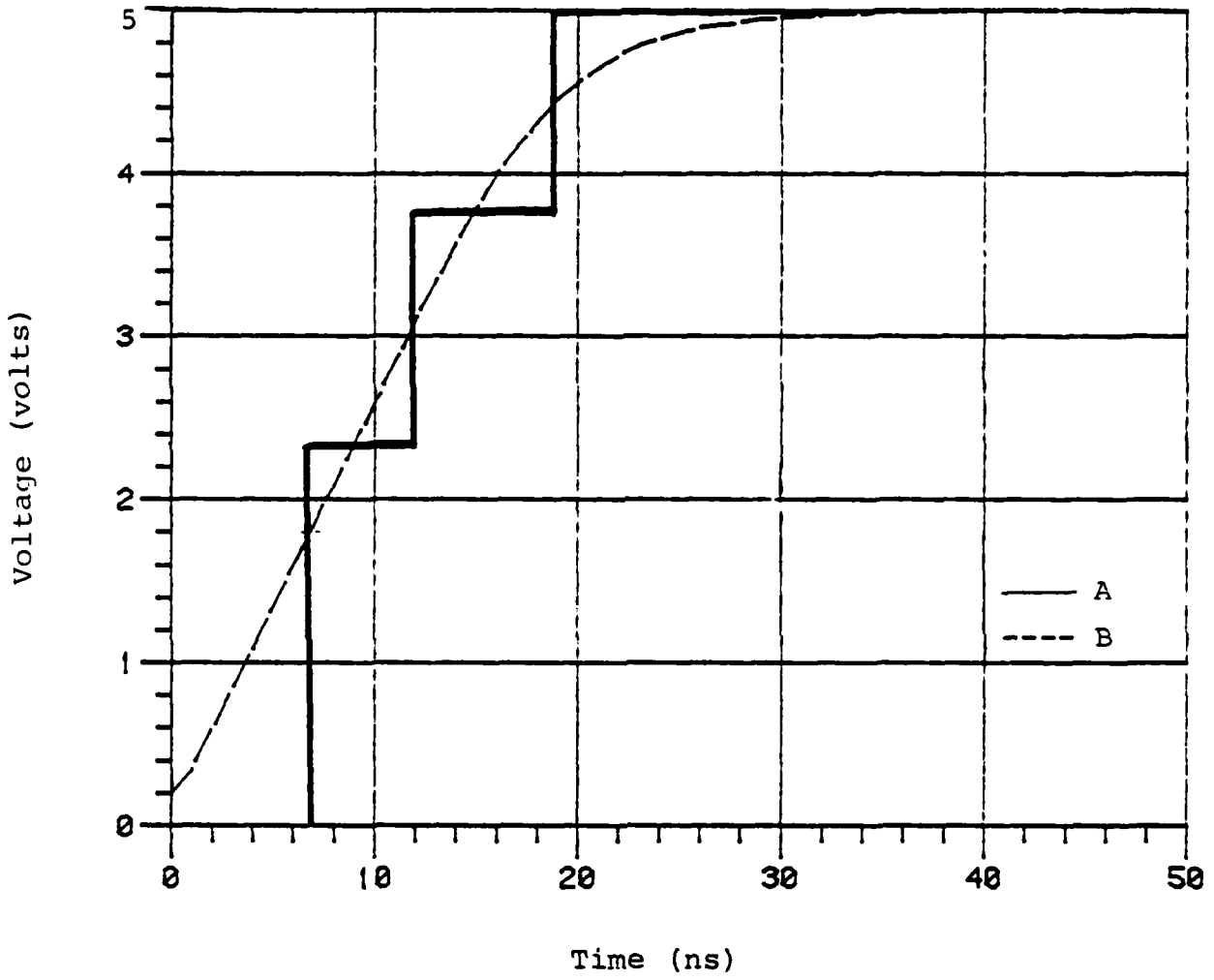
A = Discrete step function

B = Actual waveform

Fig. 5.2a. Two-step representation of waveform

short time response at the output due to large discharge current and the direct impacts on the discharge current by the input, we found that a 3-step representation as shown in Fig. 5.2b is necessary to give acceptable accuracy. Since the effective threshold voltage of the driver is 1.5 V, it was found the first sampling point for step size should be chosen at 1.8 V to produce the turn-on effect. The other sampling points will be determined by the percentage of the difference between the maximum value and the 1.8 V. If the maximum value of the input is less than or equal to 1.8 V, then the entire waveform will be represented with a step function of 1.8 V. Results with various percent points are observed. Results of the inverter chain with a step input and with the above representation are shown in Figs. 5.3a, 5.3b, 5.3c and 5.3d.

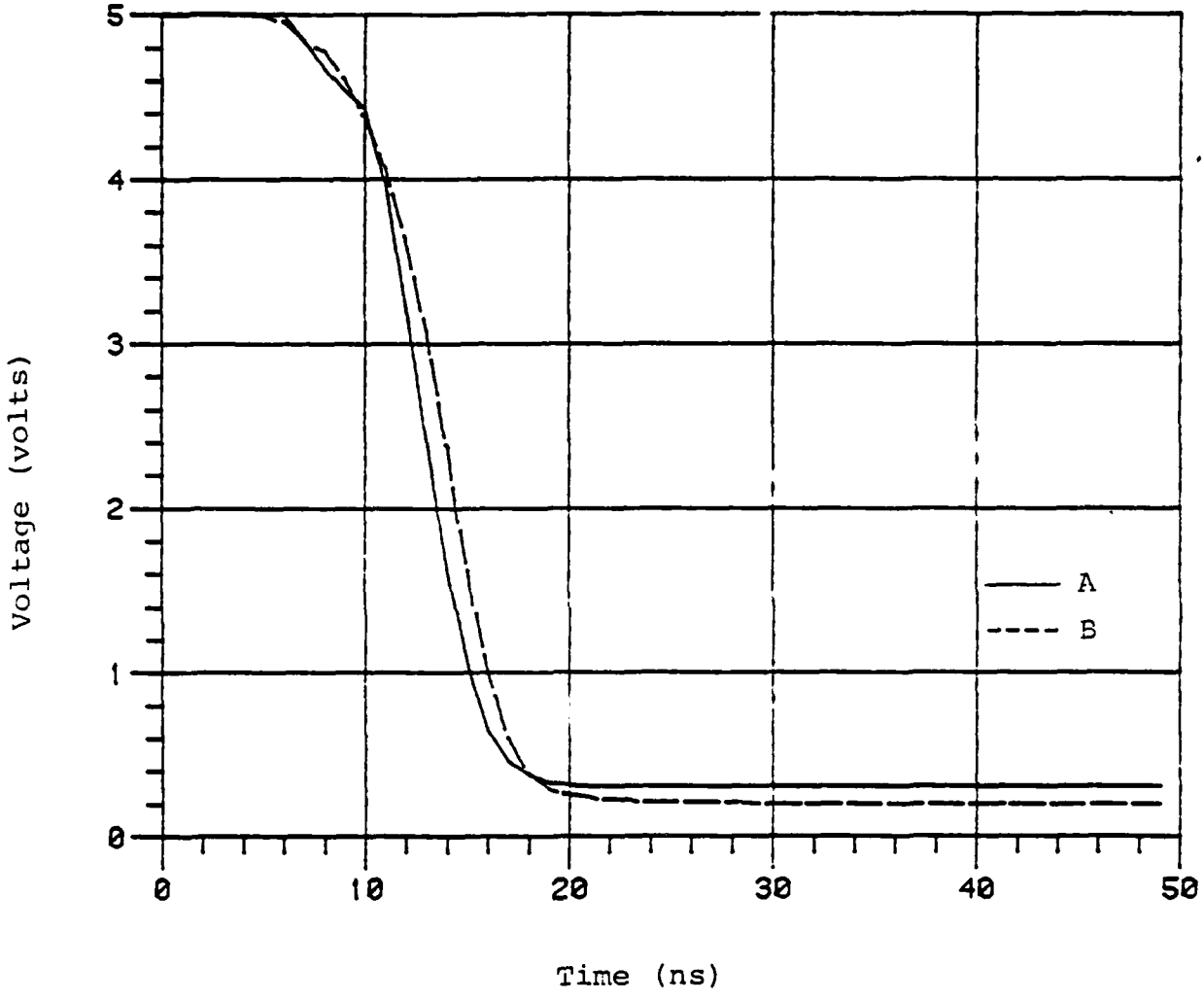
Although the step representation allows solving simple equations, a considerable amount of time is needed to set up the stepwise function. An exponential waveform is composed of segments that are defined as Eq. (4-2) at a prescribed time interval. After a sampling point for step size is determined, it is necessary to locate the corresponding segment of the waveform that contains the sampling point. After the segment is identified, Eq. (4-3) will be solved to find the step size point. The setup of the step level is trivial and straightforward. The other drawback of the step representation is the accumulated error on the delay time on the inverter chain. One advantage, however, is high-speed computation.



A = Discrete step function

B = Actual waveform

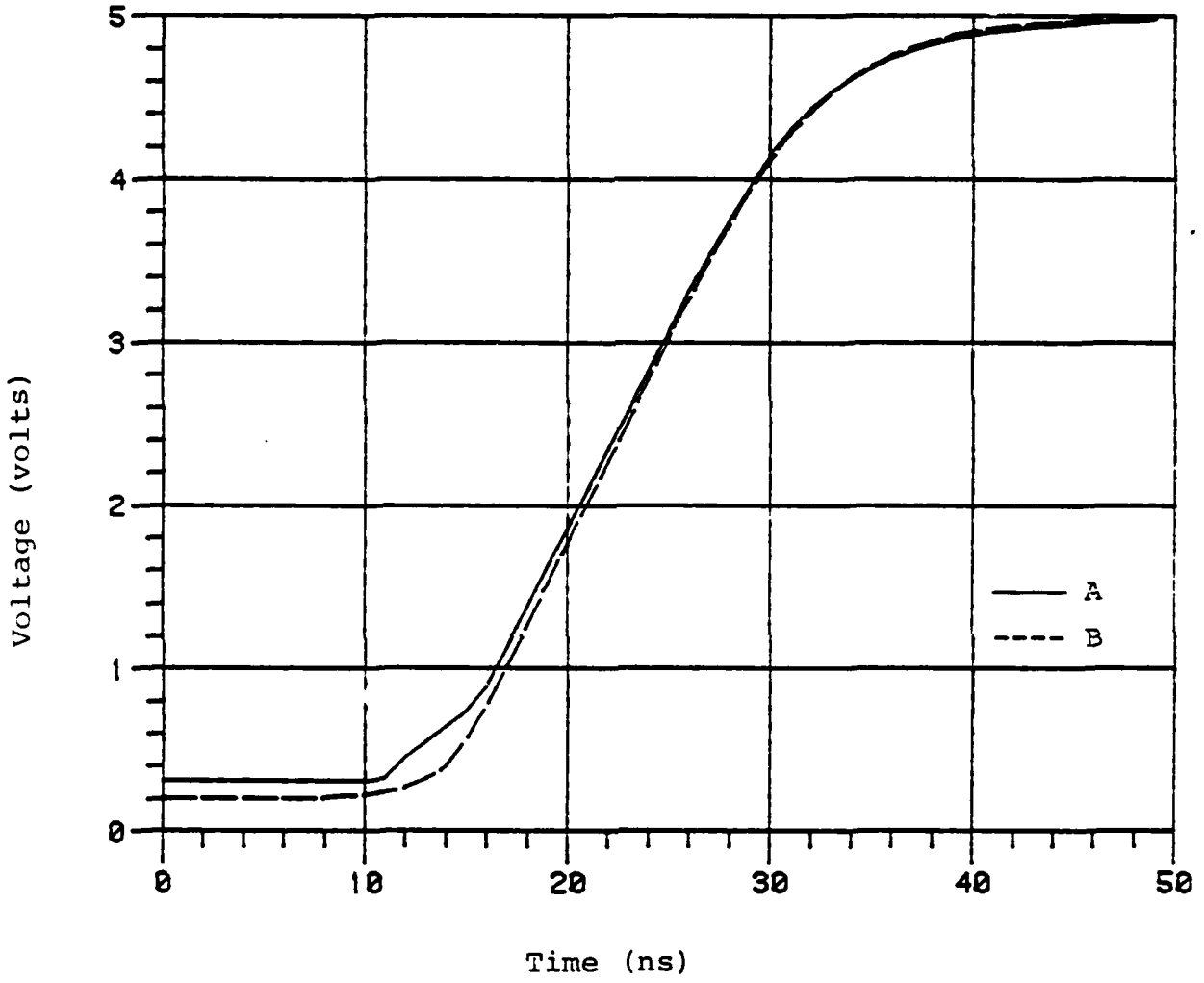
Fig. 5.2b. Three-step representation of waveform.



A = PWL model with discrete step waveform representation

B = SPICE2 output

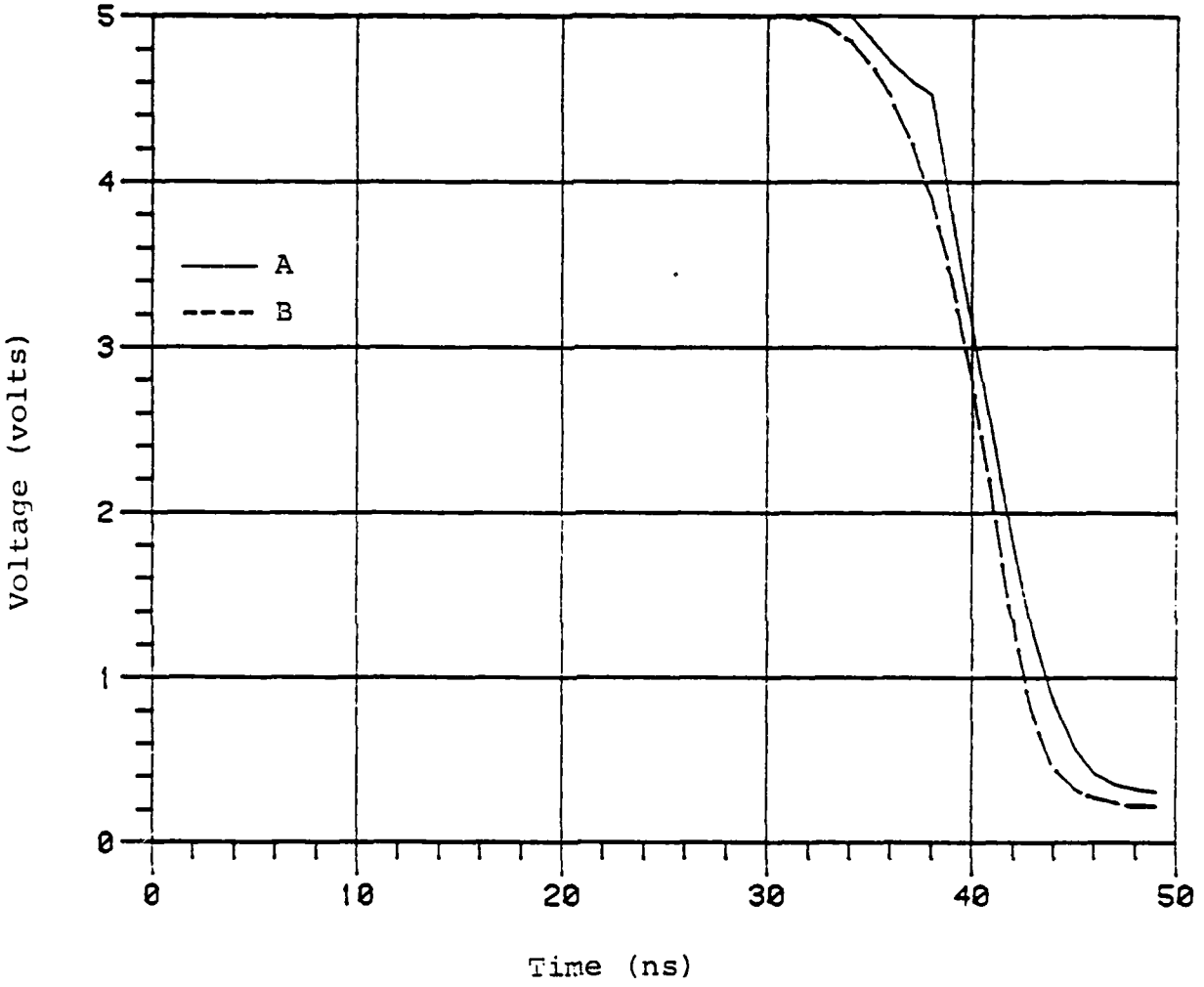
Fig. 5.3a. Output of 2nd stage.



A = PWL model with discrete step waveform representation

B = SPICE2 output

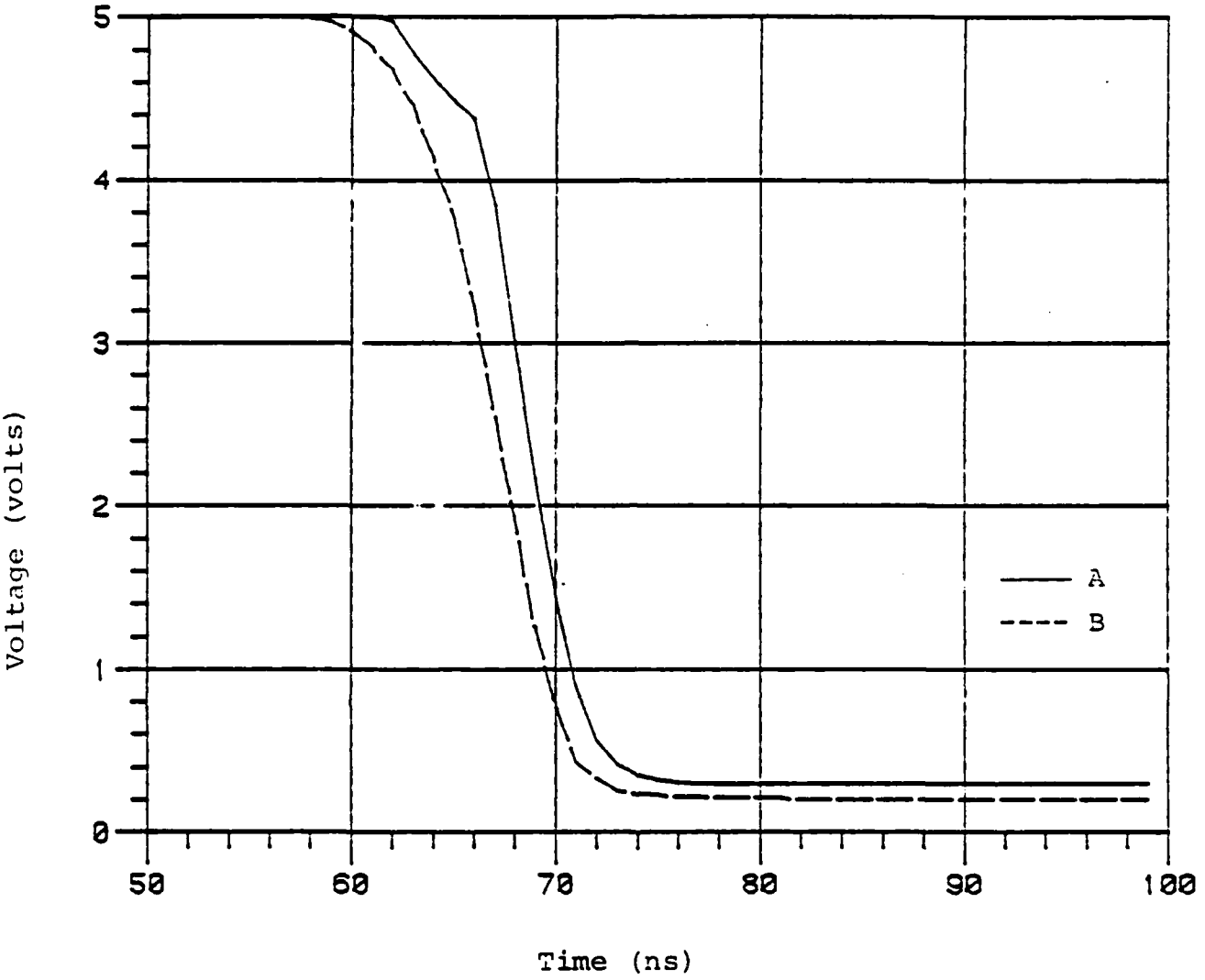
Fig. 5.3b. Output of 3rd stage.



A = PWL model with discrete step waveform representation

B = SPICE2 output

Fig. 5.3c. Output of 6^{th} stage.



A = PWL model with discrete step waveform representation

B = SPICE2 output

Fig. 5.3d. Output of 10^{th} stage.

5.3 Network with Feedback

When a circuit contains feedback, the subcircuits within the feedback loop can no longer be analyzed as a sequence of stages without iteration. The Gauss - Seidel Waveform Relaxation (WR) method [7] is chosen to decompose the circuit into several subcircuits each of which is analyzed independently as an individual stage for the entire time interval. A 3-inverter ring oscillator shown in Fig. 5.4 is used as an illustrative example.

In the oscillator circuit, instead of solving the ordinary differential equation of the form

$$\dot{X} = f(X,t) \qquad (5\text{-}3)$$

as in inverter chain, a first-order 2-dimensional differential equation with X_f as the feedback term in the form

$$\dot{X} = f(X,X_f,t) \qquad (5\text{-}4)$$

will be considered. The basic idea of the WR method is to fix all the unknown variables and solve for one variable at a time as a 1-dimensional differential equation. The solution obtained for that variable can then be substituted into another equation to solve another variable. The procedure is repeated until convergence to a solution is reached.

The step representation proposed in the last section is not practical for application in the WR method. First, in the case where the circuit is oscillatory, a lot of time is needed to set up the steps for each rising and falling edge. Second, the step representation also seems to provide

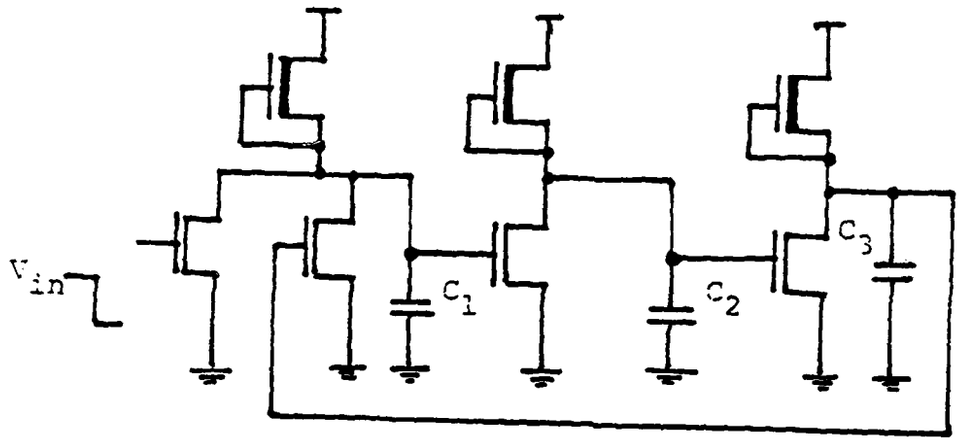


Fig. 5.4. Three inverter ring oscillator

insufficient accuracy for nonunidirectional circuits. A step representation with fixed small step size is proposed. This approach eliminates the computation of step size which can be quite time-consuming and the discrete levels of step size still allow the application of Eq. (4-2). The small step size also provides a higher degree of accuracy.

A fixed step size of 1 nsec is used. One approach to set up the step level is to take the average of the voltage levels at both ends of a step size. To simplify the analysis further, the procedure to detect the time point where the trajectory crosses a breakpoint is eliminated. Only the initial state, the equilibrium state, and time constant of Eq. (4-2) are evaluated at the endpoints. Because of the small step size, the error due to this simplification is not significant. A solution similar to Eq. (4-2) will be reproduced in terms of the stepwise input. In general, the first-order differential equation of Eq. (4-1) can be expressed as

$$\dot{x} = ax + bu + c \tag{5-5}$$

where x is the output and u is the input.

Solution of the above equation is obtained by solving

$$x(t) = x(t_o)e^{a(t-t_o)} + e^{at} \int_{t_o}^{t} e^{-a\tau}(bu(\tau)+c)d\tau \tag{5-6}$$

Let the input u be expressed as the average voltage between the endpoints of a step size as shown in Fig. 5.5.

$$u = \frac{u(t_o) + u(t)}{2} \tag{5-7}$$

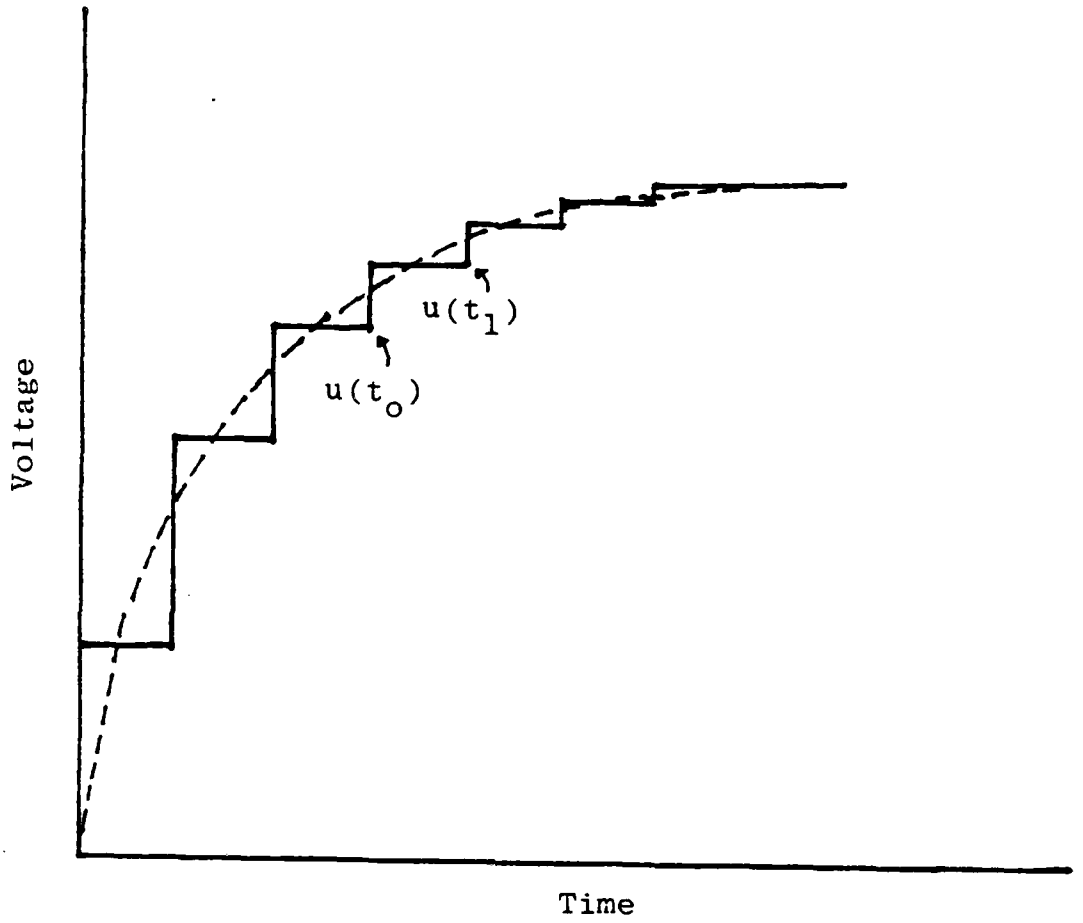


Fig. 5.5. Waveform representation with steps.

Then

$$x(t) = \left[x(t_o) - \frac{bu}{a}\right]e^{a(t-t_o)} - \frac{bu}{a} \qquad (5\text{-}8)$$

Results of the ring oscillator with the above stepwise function are shown in Fig. 5.6. Note that the convergence of the iterated solution on the oscillator is achieved with the number of iterations being proportional to the number of oscillating cycles for a given time interval.

The above step representation offers good results but the small step size requires a lot of table lookups. It is possible to eliminate some of the table lookups by replacing some of the small step sizes with a larger step size. Another approach which allows the application of variable step size is to represent the waveform by segments of ramp as shown in Fig. 5.7.

Solution of Eq. (5-6) with the ramp function involves solving the trapezoidal area under the curve and it is given by

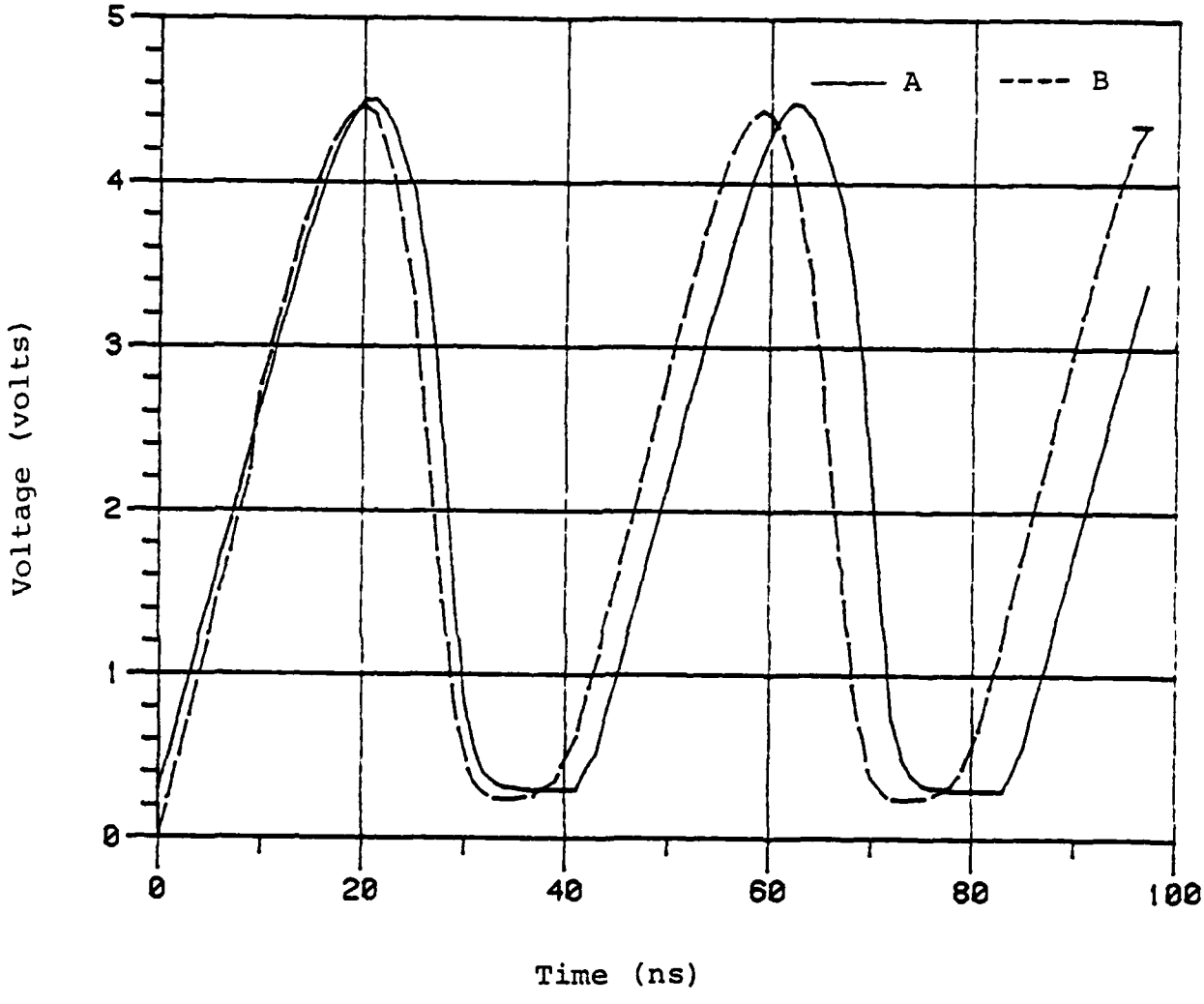
$$x(t) = \left[x(t_o) + \frac{bu(t_o) + c}{2}(t-t_o)\right] e^{a(t-t_o)} + \frac{bu(t)+c}{2}(t-t_o) \qquad (5\text{-}9)$$

for $t_o \leq t \leq t+h$

where $a = \frac{1}{RC}$

$h = t_1 - t_o$ is the step size.

At the endpoint $t = t_1$ of a step



A = Waveform representation by step and WR method

B = SPICE2 output

Fig. 5.6. Output of the 1st inverter in the three inverter ring oscillator.

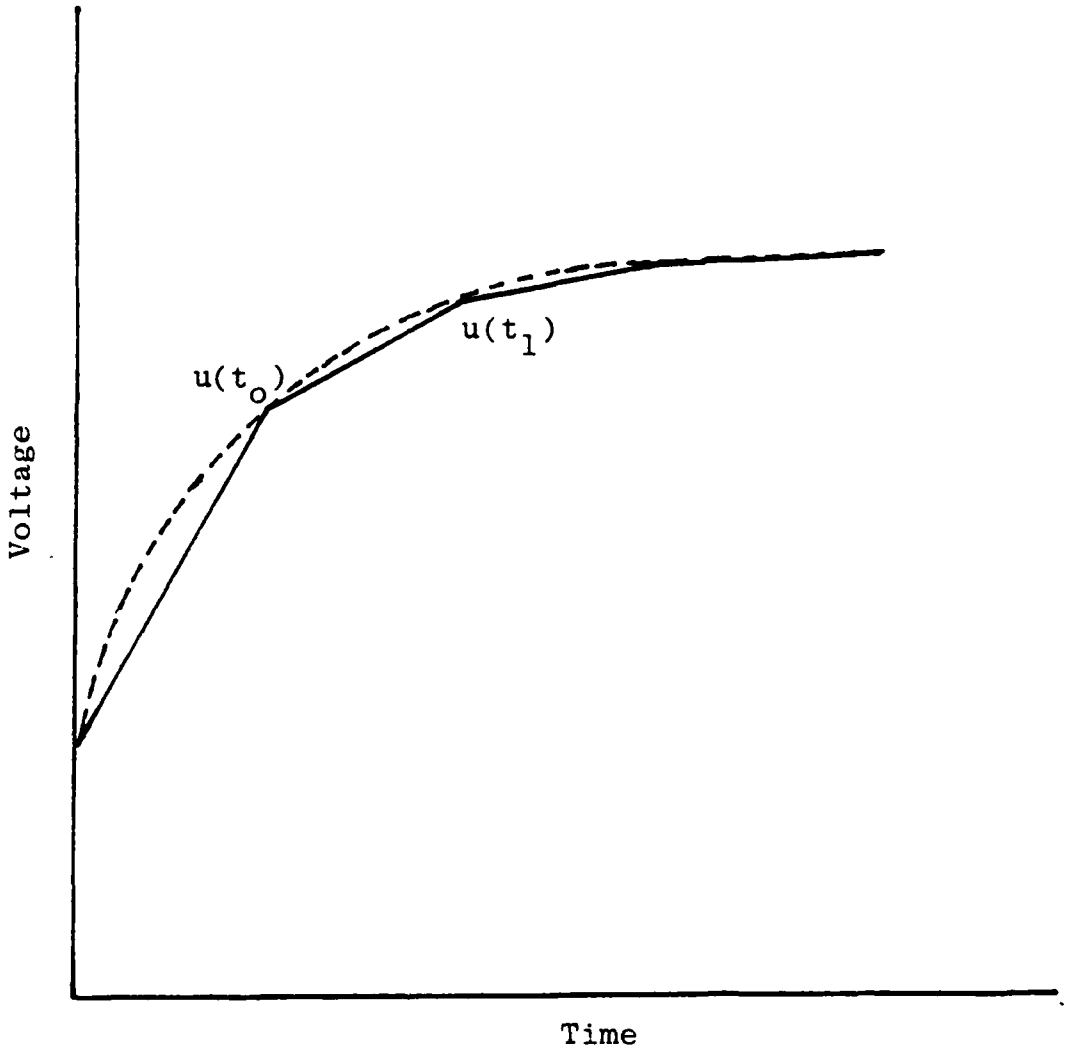


Fig. 5.7. Waveform representation with ramp.

$$x(t_1) = \left[x(t_o) + \frac{bu(t_o)+c}{2} * h \right] e^{ah + \frac{bu(t_1)+c}{2} * h} \qquad (5\text{-}10)$$

If the difference between $u(t_o)$ and $u(t_1)$ is small, the step size h can be increased without degrading the accuracy. On the other hand, the step size can be decreased to improve accuracy. Results from the ramp representation with fixed step size shown in Fig. 5.8 are almost identical to those in Fig. 5.6.

The technique applied to check for convergence compares the values of the iterated solutions at the end of the given time interval. The results indicate this method of checking for convergence is quite efficient and reliable.

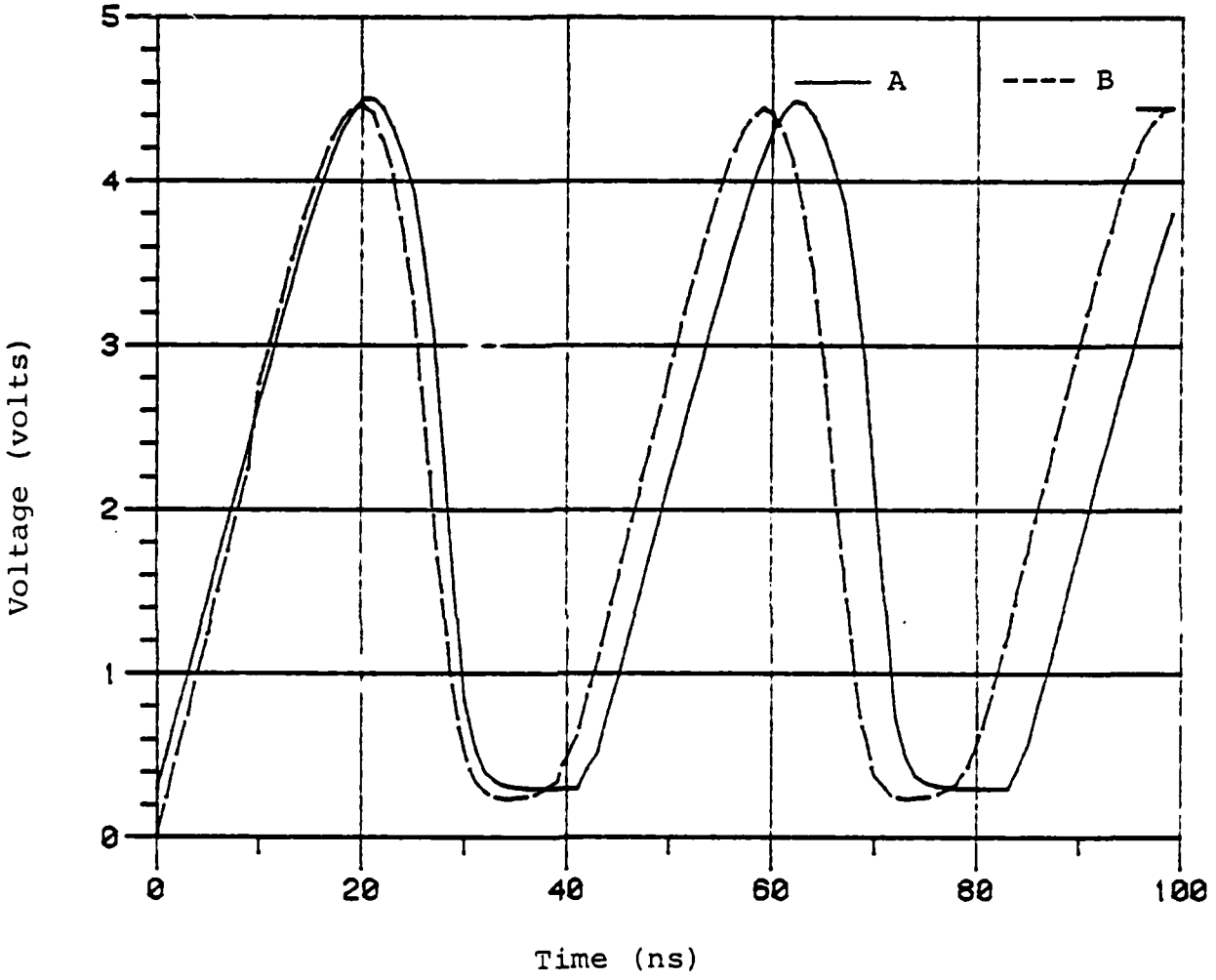
5.4 Network with Pass Transistor

The circuit shown in Fig. 5.9 is a basic part of the common dynamic shift register. The PWL model of the circuit is shown in Fig. 5.10. This circuit has a coupling effect when the clock control V_{CLK} of the pass transistor is on and both C_1 and C_2 are charging and discharging at the same time. The circuit can be described by a first-order 2-dimensional differential equation of the following form:

$$\dot{V}_{C_1} = M_1 V_{C_1} + M_2 V_{C_2} + M_3 * V_{CLK} + M_4 * V_{in} + M_9 \qquad (5\text{-}11a)$$

$$\dot{V}_{C_2} = M_5 V_{C_1} + M_6 V_{C_2} + M_7 * V_{CLK} + M_8 \qquad (5\text{-}11b)$$

The Gauss-Seidel WR method will be used again to solve these equations as two 1-dimensional differential equations.



A = waveform representation by ramp and WR method

B = SPICE2 output

Fig. 5.8 Output of the 1st inverter in the three inverter ring oscillator.

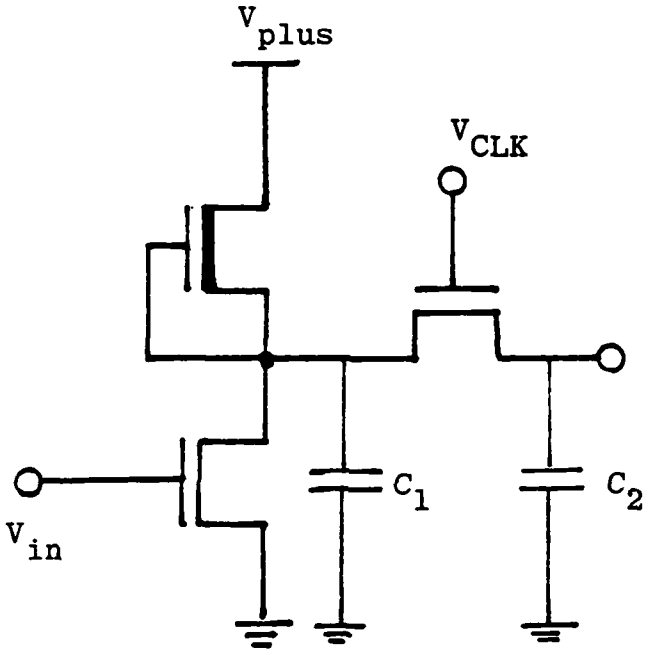


Fig. 5.9. Test circuit.

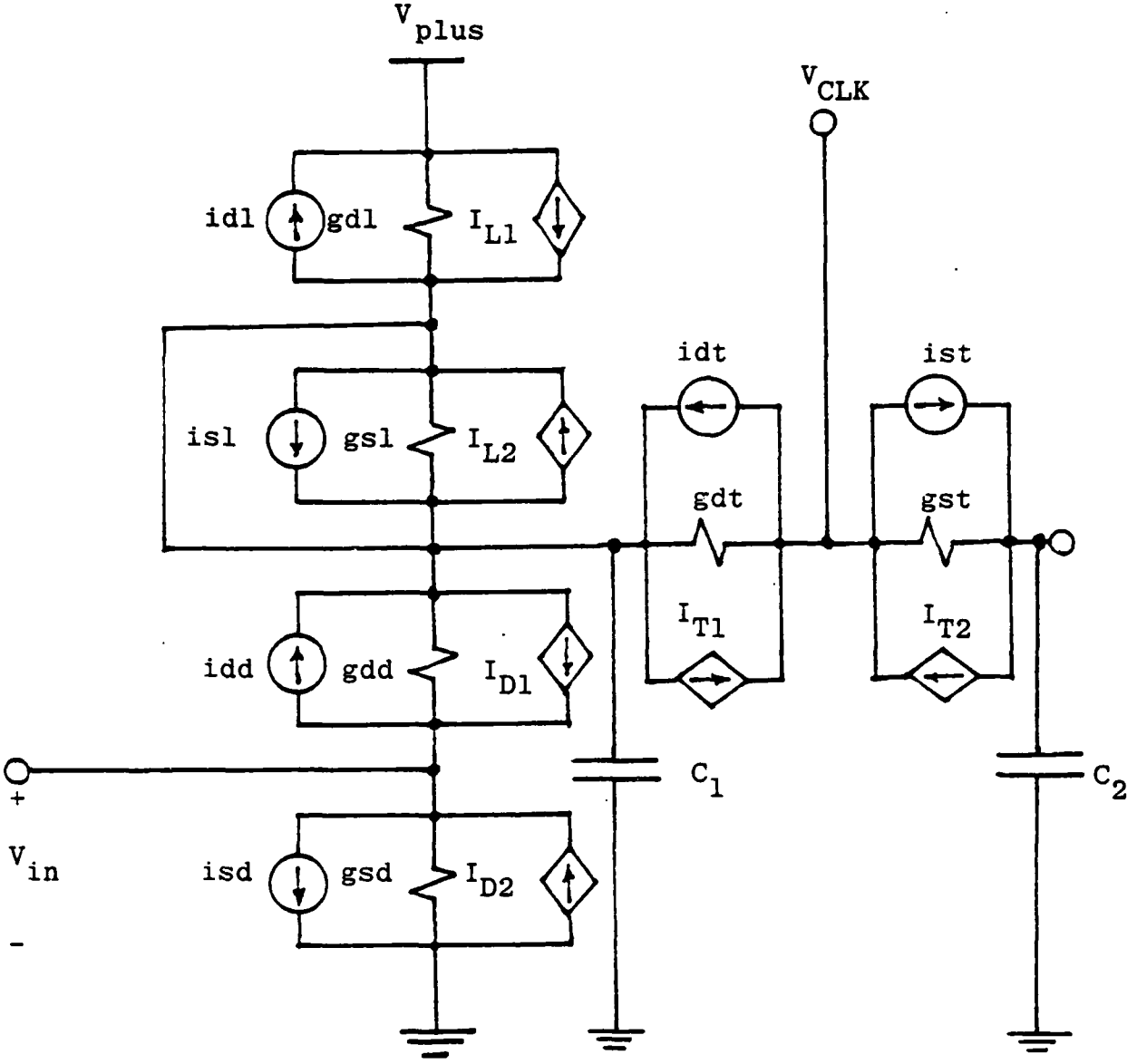


Fig. 5.10. PWL model of Fig. 5.9.

Taking KCL at the output terminal of the inverter gives the following expression.

$$C1\frac{dV_{C1}}{dt} + I_{D1} + I_{T1} + Vgd1*id1 + id1 - I_{L1} - Vgdd*gdd - id - Vgdt*gdt - id t = 0 \qquad (5\text{-}12)$$

where $I_{D1} = Vgsd*gsd + isd$

$I_{L1} = Vgsl*gsl + isl$

$I_{T1} = Vgst*gst + ist$

$Vgd1 = V_{C1} - V_{plus}$

$Vgdd = V_{in} - V_{C1}$

$Vgdt = V_{CLK} - V_{C1}$

$Vgsd = V_{in}$

$Vgst = V_{CLK} - V_{C_2}$

$Vgsl = 0$

Rearrangement of Eq. (5-12) gives the Norton equivalent form of Eq. (4-2) with the following values for the elements:

$$R = \frac{1}{gd1+gdd+gdt} \qquad (5\text{-}13)$$

$$I_s = K_1 + K_2*V_{in} + K_3*V_{C2} + K_4*V_{CLK} \qquad (5\text{-}14)$$

where K_1 = (isl-idl) + (idd-isd) + (idt-ist) + V_{plus}*gdl

K_2 = gdd - gsd

K_3 = gst

K_4 = gdt - gst

Substituting Eq. (5-13) and Eq. (5-14) into Eq. (5-12) gives an equivalent form of Eq. (5-11a) which is also used as the basic circuit equation for the WR method. Taking another KCL equation at V_{C2} gives

$$C2 \frac{dV_{C2}}{dt} + Vgst*gst + ist - I_{T2} = 0 \qquad (5\text{-}15)$$

where I_{T2} = Vgdt*gdt + idt

Vgst = V_{CLK} - V_{C2}

Vgdt = V_{CLK} - V_{C1}

Rearrangement of Eq. (5-15) gives the Norton equivalent form of Eq. (4-2) with the following values for the elements:

$$R = \frac{1}{gst} \qquad (5\text{-}16)$$

$$I_s = K_5 + K_6*V_{C1} + K_7*V_{CLK} \qquad (5\text{-}17)$$

where K_5 = ist - idt

K_6 = gdt

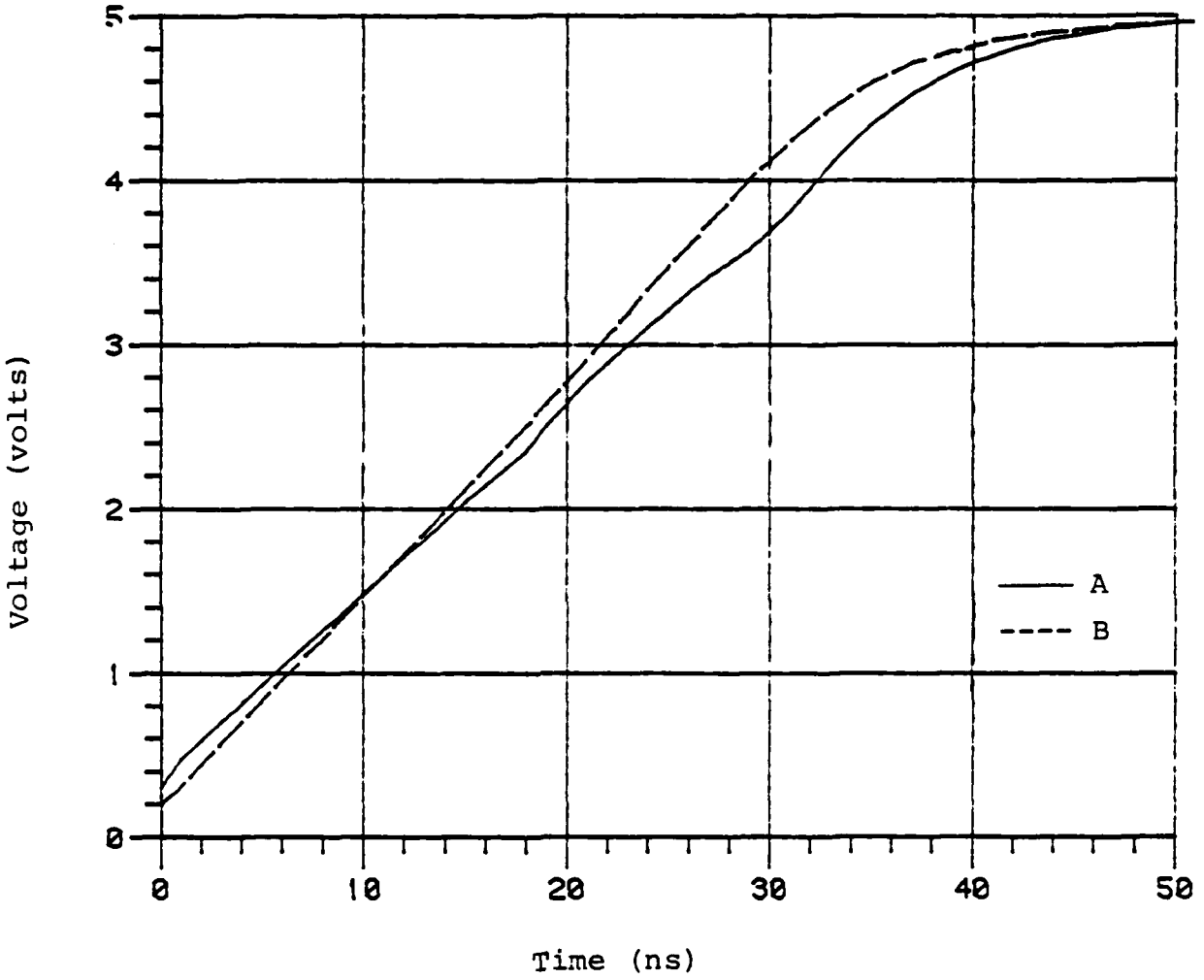
K_7 = gst - gdt

Substituting Eq. (5-16) and Eq. (5-17) into Eq. (5-15) gives an equivalent form of Eq. (5-11b) which is the basic circuit equation for the WR method.

The delay through such a circuit is different from the inverter delay which is more dependent on the input level. In the case where both capacitors are charging up, the results by the WR method show a slower time response than those of SPICE2. The major reason is the larger effective threshold voltage of the pass transistor gives lower steady-state values for V_{C2}. Since V_{C1} is coupled to V_{C2}, both V_{C1} and V_{C2} have significantly longer rise times than the SPICE2 output. The results are shown in Fig. 5.11.

5.5 Convergence Problem of Waveform Relaxation Method

The bootstrap circuit in Fig. 5.12 has a floating capacitor C_b as the feedback element. The WR method and stepwise function are applied to analyze this circuit. If the value of C_b is relatively large, then the solution does not converge. A much smaller step size is necessary to analyze this problem. The simulated results with C_b = 0.005 pF and the other output capacitors at 0.1 pF are shown in Figs. 5.13a,b, c, where it can be seen that the result by this approach is not accurate in comparison with SPICE2.



A = A waveform representation by step and WR method

B = SPICE2 output

Fig. 5.11. Output of inverter at the pass transistor network.

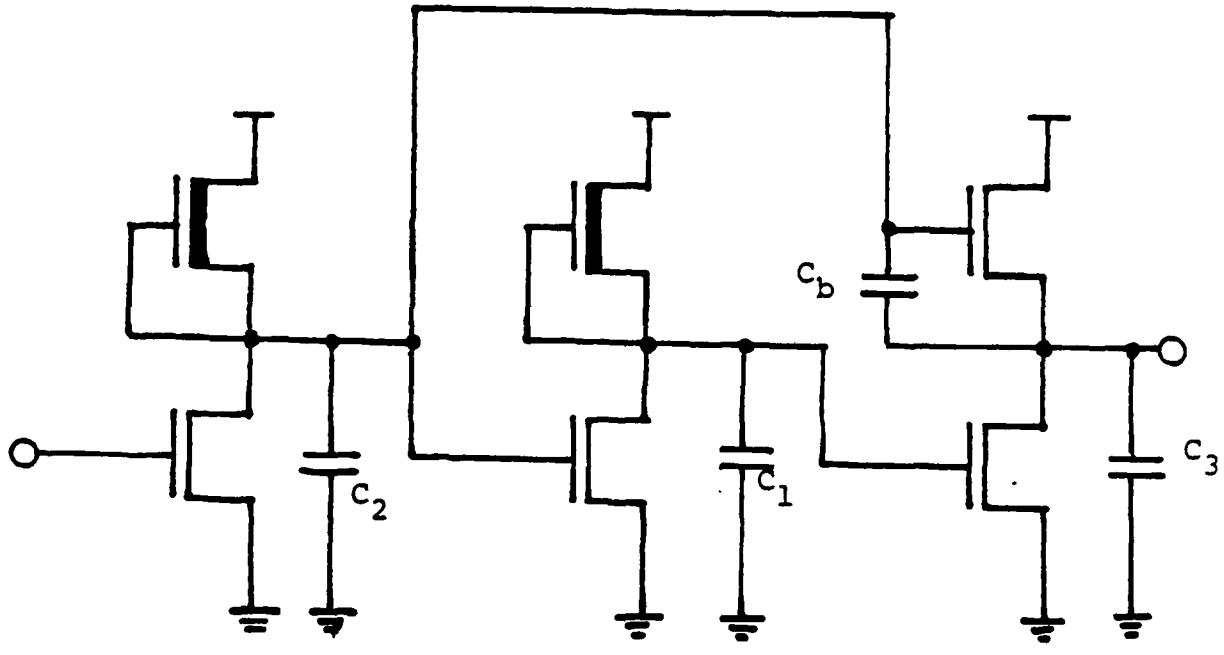
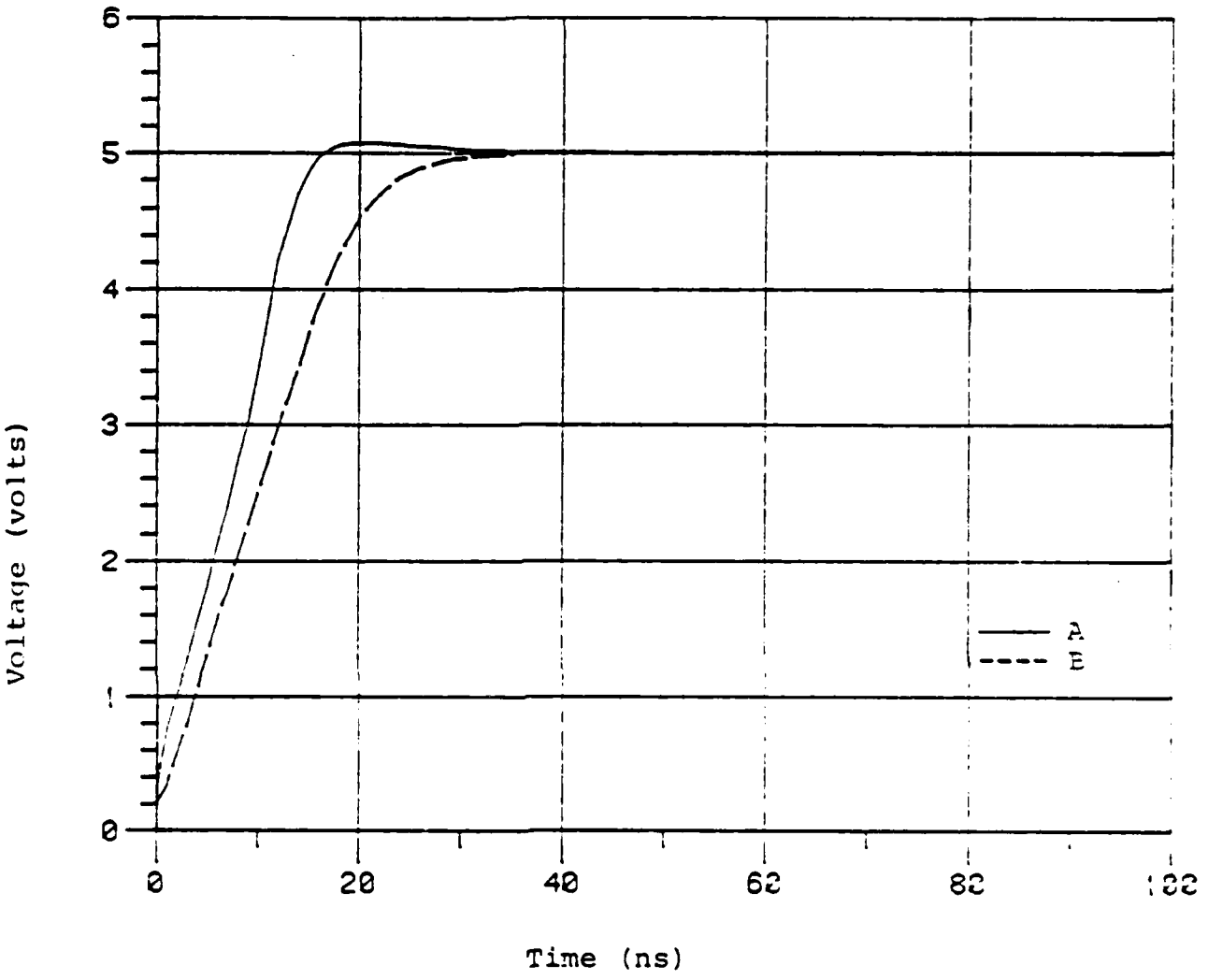


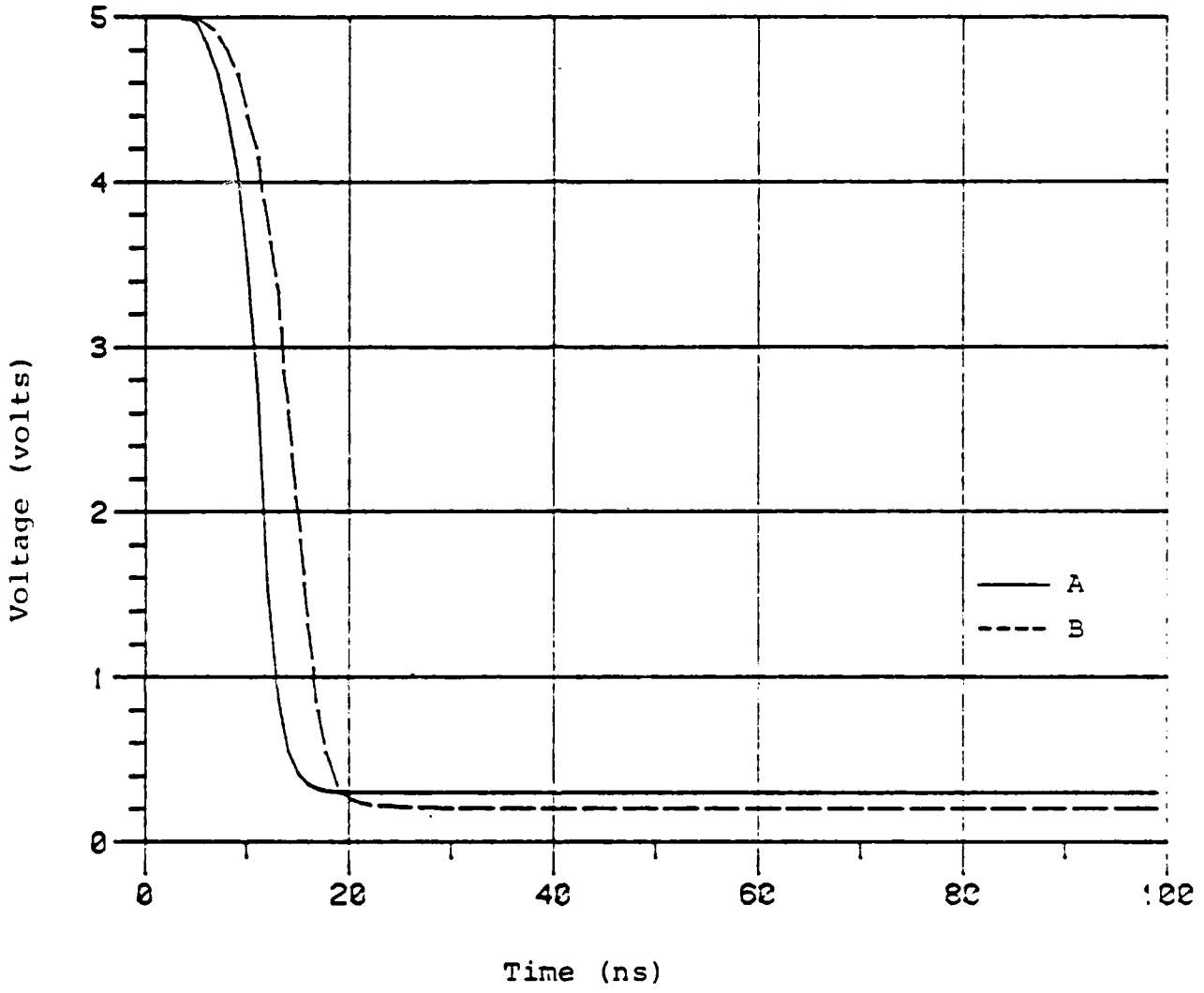
Fig. 5.12. Bootstrap capacitor circuit.



A = A waveform representation by step and WR method

B = SPICE2 output

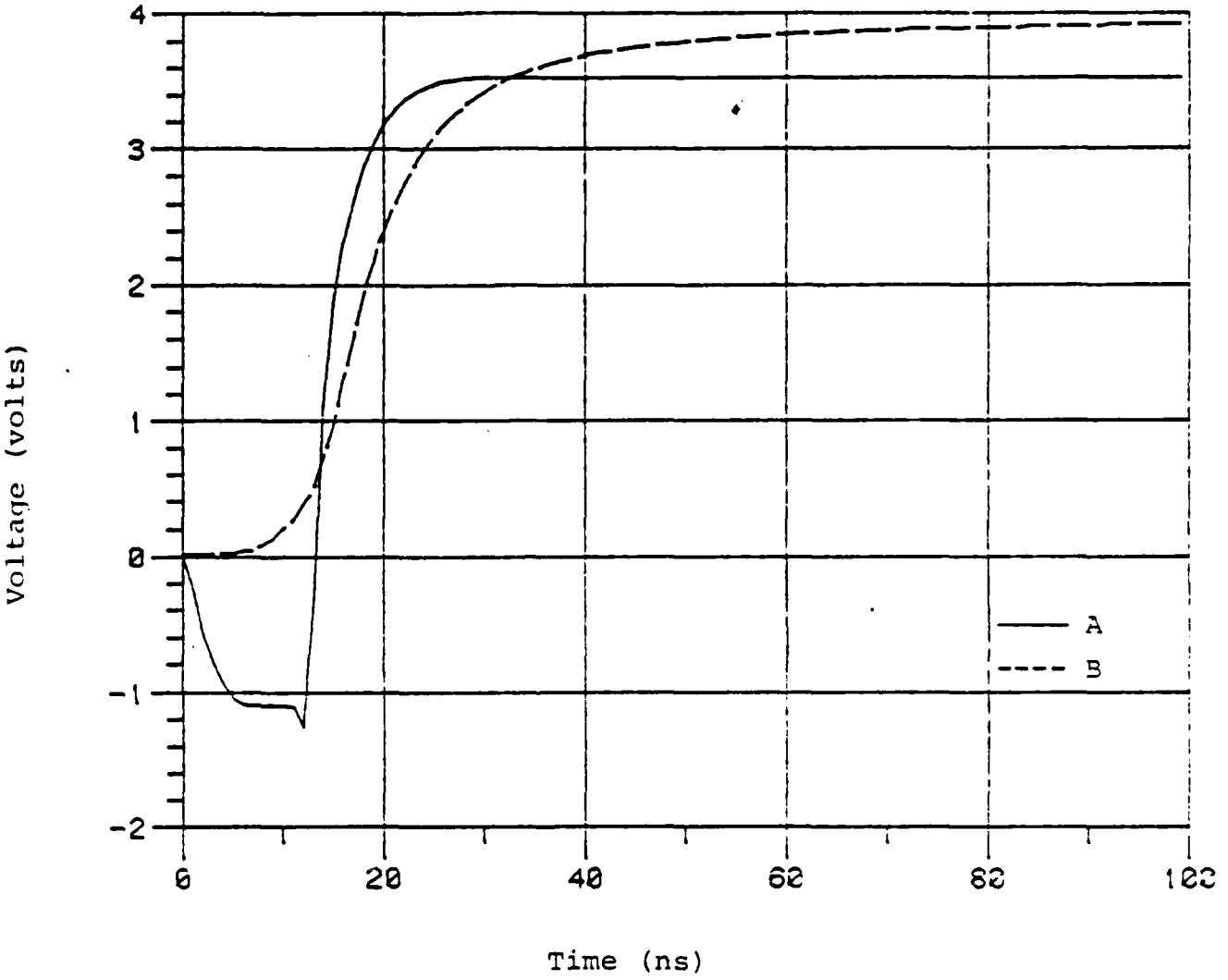
Fig. 5.13a. Output of 1st inverter in the bootstrap circuit.



A = A waveform representation by step and WR method

B = SPICE2

Fig. 5.13b. Output of 2nd inverter in the bootstrap circuit.



A = A waveform representation by step and NR method

B = SPICE2

Fig. 5.13c. Output of 3rd inverter in the bootstrap circuit.

Chapter 6

CONCLUSION

A PWL model of MOS transistor circuits has been constructed. The aim of this model is to provide acceptable accuracy without solving complex nonlinear equations. A configuration of interconnection of 2-terminal nonlinear elements for the MOS is used. This form not only satisfies the requirement of the PWL canonic form but also allows the application of 1-dimensional table lookups. In addition, more memory saving is achieved because the completely bi-directional property of the model requires only one table to represent both nonlinear elements.

Two approaches to function generation by PWL segments have been studied. Both approaches are convenient and easy to implement. For accuracy measurements of the approximation, the Katzenelson algorithm is used to study the DC characteristics of the depletion-load inverter. The first approach uses chord approximation. The advantage of this approach is the exact representation of the i-v curve at the threshold voltage and the straightforward setup of the chords. However, it suffers from accuracy problems if the DC operating point is placed near the maximum error point. The DC output also exhibits high dependence on the endpoint of the chords. The second approach is the tangent approximation. It is slightly more complicated to set up; however, the error has been reduced significantly. Even with the DC operating

point at the maximum error point, the results still provide good accuracy. The major drawback to this approach is the variation of the threshold voltage sometimes imposes a problem on timing analysis.

For the understanding of the model's transient behavior, step inputs were applied to the inverter and 2-input NAND gate for observation. The values of the step function are selected such that the impacts of the load and driver on the output can be separated. Thus, each transistor's model parameters can be examined to determine the best PWL segment approximation. Although the changes of threshold voltages due to tangent approximation contribute to errors in the transient analysis, the results are considered acceptable. The solutions of the PWL model in the 2-input NAND gate circuit with various inputs display accuracy that is as good as the solution in the inverter.

The PWL approach allows a PWL model network to be transformed into a first-order dynamic network in a given segment. The solution of this simple equivalent circuit with constant input leads to an exponential waveform or linear waveform, whose exact form can be found by determining only three pieces of information, namely, the initial state, the equilibrium state, and the time constant associated with the segment. This information is easily obtained by employing the table lookup method.

For realistic circuit analysis, the exponential waveform is considered. A discrete stepwise function is proposed to

represent the exponential waveform. First, this representation avoids solving the nonlinear equations. Second, it adopts the simple solution for constant input which can be solved easily with table lookup. A 10-stage inverter chain is used to illustrate the effectiveness of the stepwise representation. The outputs at various stages are observed to give a good approximation quickly. Although the discrete representation enjoys solving simple equations, a considerable amount of time is needed to set up the stepwise function. The errors associated with delay time are considered large.

The effect of feedback in a circuit is studied with the application of the WR method. Two representations of waveforms are proposed to be incorporated into the WR method. The first waveform representation method is a stepwise function with small fixed step size. The analysis of this representation is treated as constant input at prescribed intervals. The small fixed step size eliminates the computation of step size and gives very good accuracy. However, the small step size requires a lot of table lookup. The second representation method is a ramp function which allows the application of variable step size. It can result in less table lookup or more accuracy as described. The analysis of this function is not more difficult than for the step case because both solutions are expressed in the same form and can be solved easily with table lookup.

The WR method with small step size stepwise representation was also applied to solve the network with a pass

transistor. The result exhibits significantly slower response on the turn-off case. The major reason is the larger effective threshold voltage of the pass transistor gives lower steady-state value. The study of the bootstrap circuit indicates the WR method will not be convergent when a strong feedback element exists.

The simulation data of the following cases which were analyzed in the previous sections with the waveform relaxation and small fixed step size stepwise representation are compared with those obtained from SPICE2.

Case 6.1: The 3-inverter ring oscillator in Fig. 5.4.

Case 6.2: The pass transistor network in Fig. 5.9.

Case 6.3: The bootstrap circuit in Fig. 5.12.

The other example used the variable level discrete steps for waveform representation.

Case 6.4: The ten-stage inverter chain in Fig. 5.1.

These simulation data shown in Table 6.1 indicate the PWL approach provides some savings in CPU time. However, some examples also illustrate accuracy or convergence problems. A modified version of the WR method or a total new approach should be investigated to overcome the problems. A different set of PWL segments may be necessary to represent a pass transistor. The waveform representation by ramp functions should be developed in more detail to implement variable step size.

Table 6.1

SIMULATION DATA BY PWL APPROACH AND SPICE2

Case	PWL Approach	SPICE2	Saving in CPU Times
6.1	2.52 sec	16.1 sec	84.3%
6.2	2.78 sec	6.50 sec	57.2%
6.3	2.05 sec	12.2 sec	83.2%
6.4	2.22 sec	42.7 sec	94.8%

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